EXHIBIT 8

United States Patent [19]

Beckner et al.

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[45] **Date of Patent: Apr. 4, 1989**

[54] **FRAMER CIRCUIT FOR USE IN A DTDM NETWORK**

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[73] Assignee: **Bell Communications Research, Inc.**, Livingston, N.J.

[21] Appl. No.: **118,898**

[22] Filed: **Nov. 10, 1987**

[51] **Int. Cl.**[4] **H04J 3/02**

[52] **U.S. Cl.** **370/55**; 370/60; 370/58

[58] **Field of Search** 370/58, 55, 60, 67, 370/110.1, 84, 102, 105

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W. W. Chu, "A Study of Asynchronous Time Division Multiplexing for Time Sharing Computer Systems", Proc AFIPS, vol. 35, pp. 669–678, 1969.

A. Thomas et al., "Asynchronous Time Division Techniques: An Experimental Packet Network Integrating Video Communication", Proc International Switching Symposium, May 1984.

Primary Examiner—M. H. Paschall
Attorney, Agent, or Firm—James W. Falk

[57] **ABSTRACT**

A framer circuit which may be implemented as a single chip is disclosed. The framer circuit performs a number of functions in a DTDM network including generating trains of empty DTDM frames, enabling the writing of data packets into specific DTDM frames and the examination of header data in specific DTDM frames to generate signals for the control of peripheral circuits. The framer circuit comprises an input serial/parallel converter, a frame detection circuit, an output parallel/serial converter and a control unit comprising one or more finite state machines for generating proper control signals such as read and write strobes for data insertion and extraction.

14 Claims, 10 Drawing Sheets

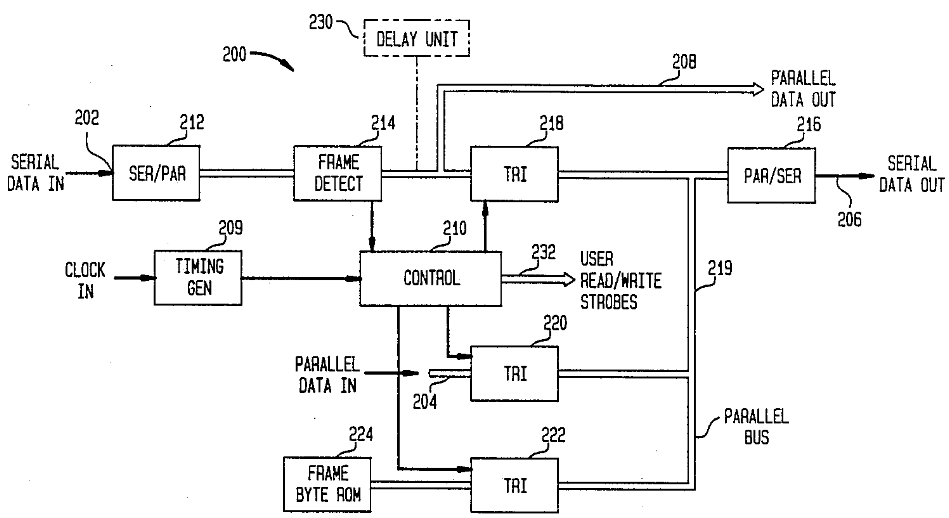


FIG. 1

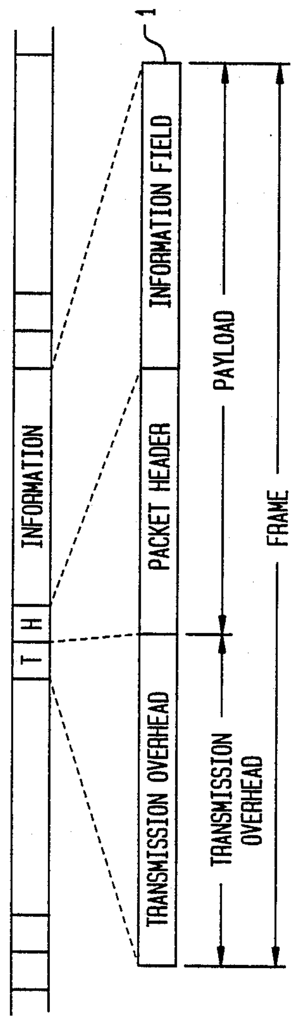

INFORMATION
T
H
1
INFORMATION FIELD
PACKET HEADER
TRANSMISSION OVERHEAD
PAYLOAD
TRANSMISSION OVERHEAD
FRAME

FIG. 2

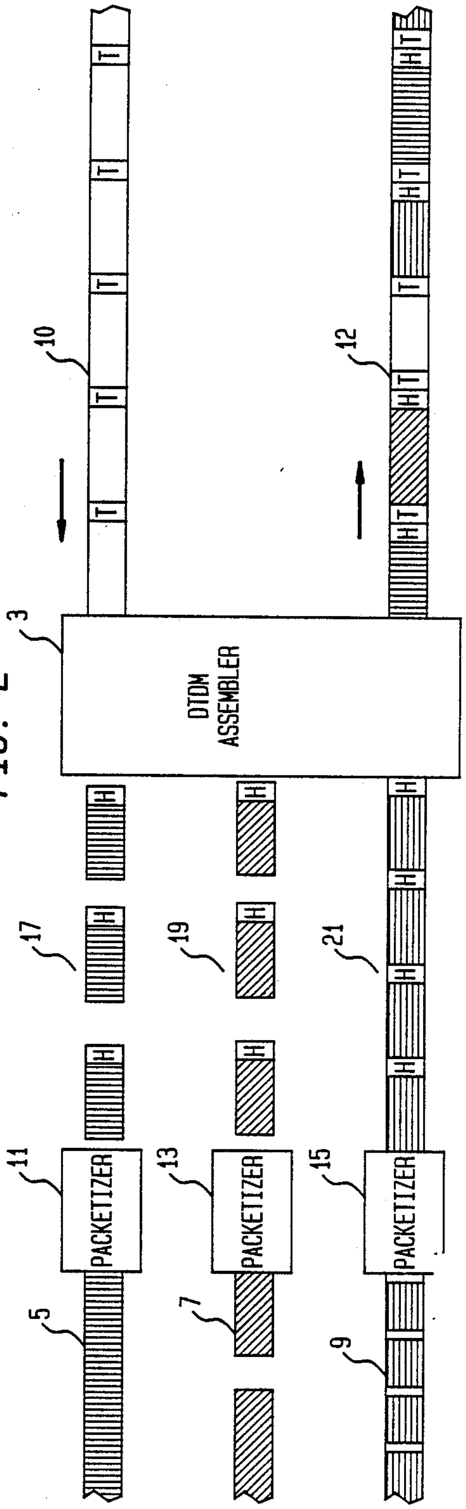
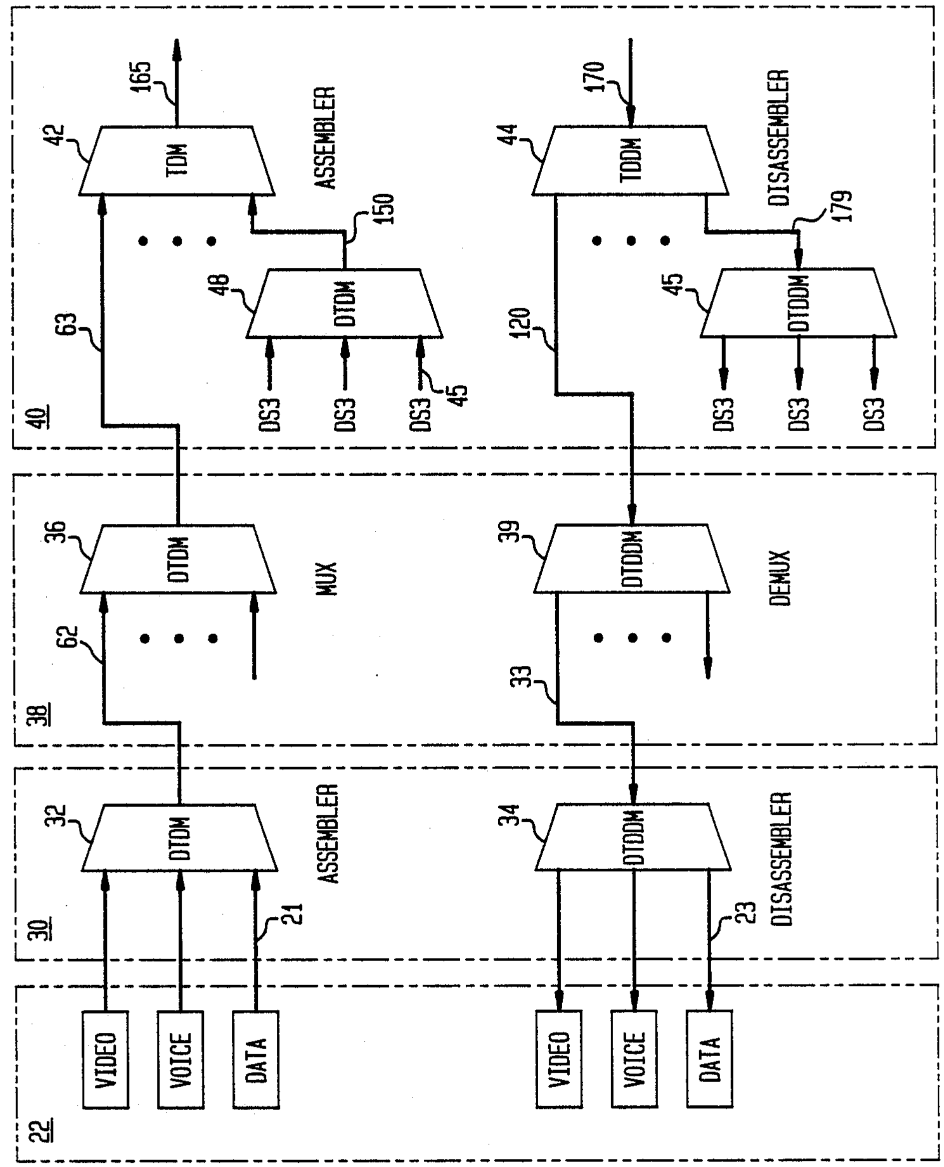

10
12
3
DTDM ASSEMBLER
17
19
21
11
13
15
PACKETIZER
PACKETIZER
PACKETIZER
5
7
9

FIG. 3

20


40
TDM
ASSEMBLER
DTDM
DS3
DS3
DS3
TDDM
DISASSEMBLER
DTDDM
DS3
DS3
DS3
38
DTDM
MUX
DTDDM
DEMUX
30
DTDM
ASSEMBLER
DTDDM
DISASSEMBLER
22
VIDEO
VOICE
DATA
VIDEO
VOICE
DATA

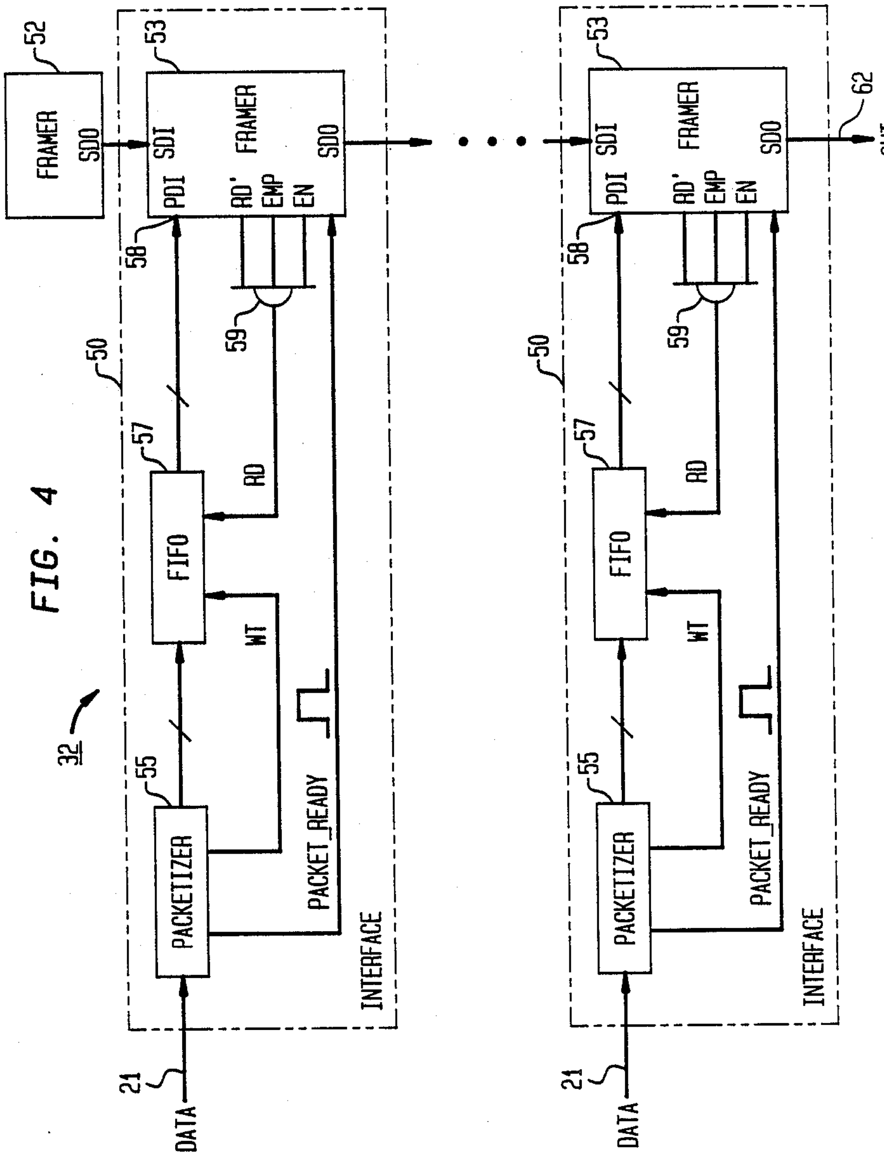

32
52
FRAMER
SDO
50
53
SDI
FRAMER
PDI
RD'
EMP
EN
SDO
58
59
57
FIFO
RD
WT
55
PACKETIZER
PACKET_READY
INTERFACE
21
DATA
50
53
SDI
FRAMER
PDI
RD'
EMP
EN
SDO
62
OUT
58
59
57
FIFO
RD
WT
55
PACKETIZER
PACKET_READY
INTERFACE
21
DATA

FIG. 4

FIG. 5

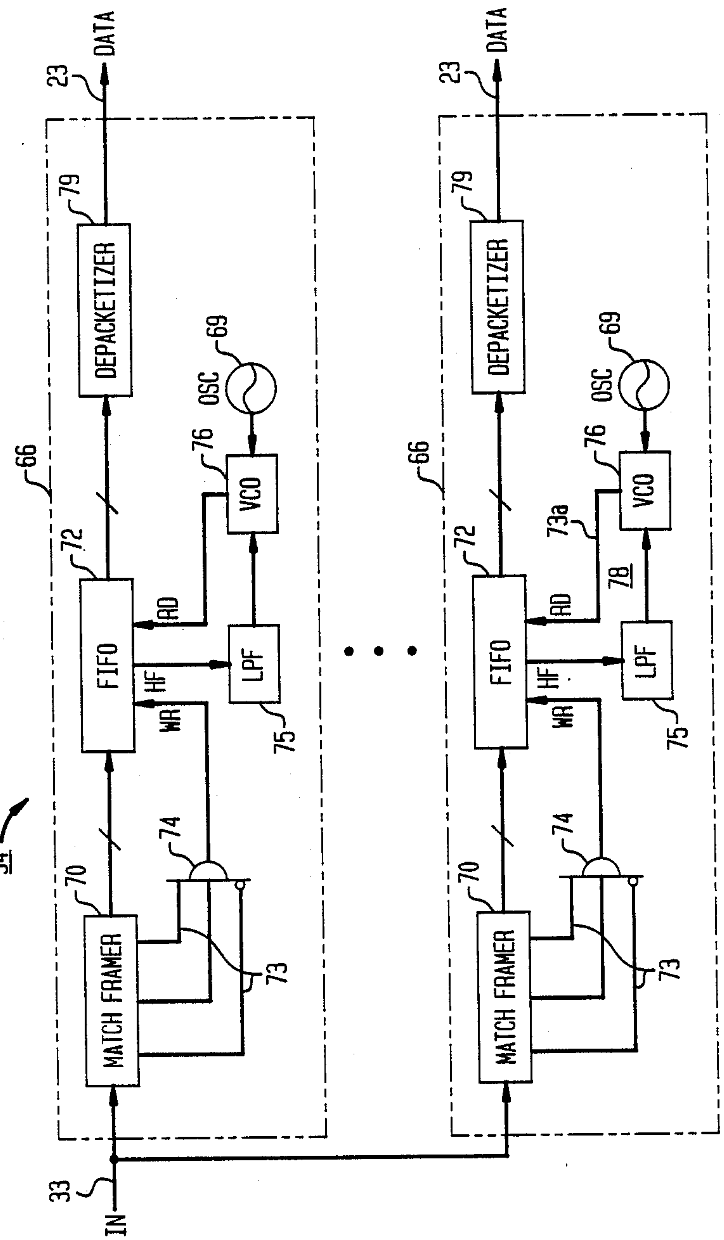

34
DATA
23
79
DEPACKETIZER
66
69
OSC
76
VCO
72
FIFO
RD
HF
WR
LPF
75
73a
78
74
70
MATCH FRAMER
73
33
IN

FIG. 6

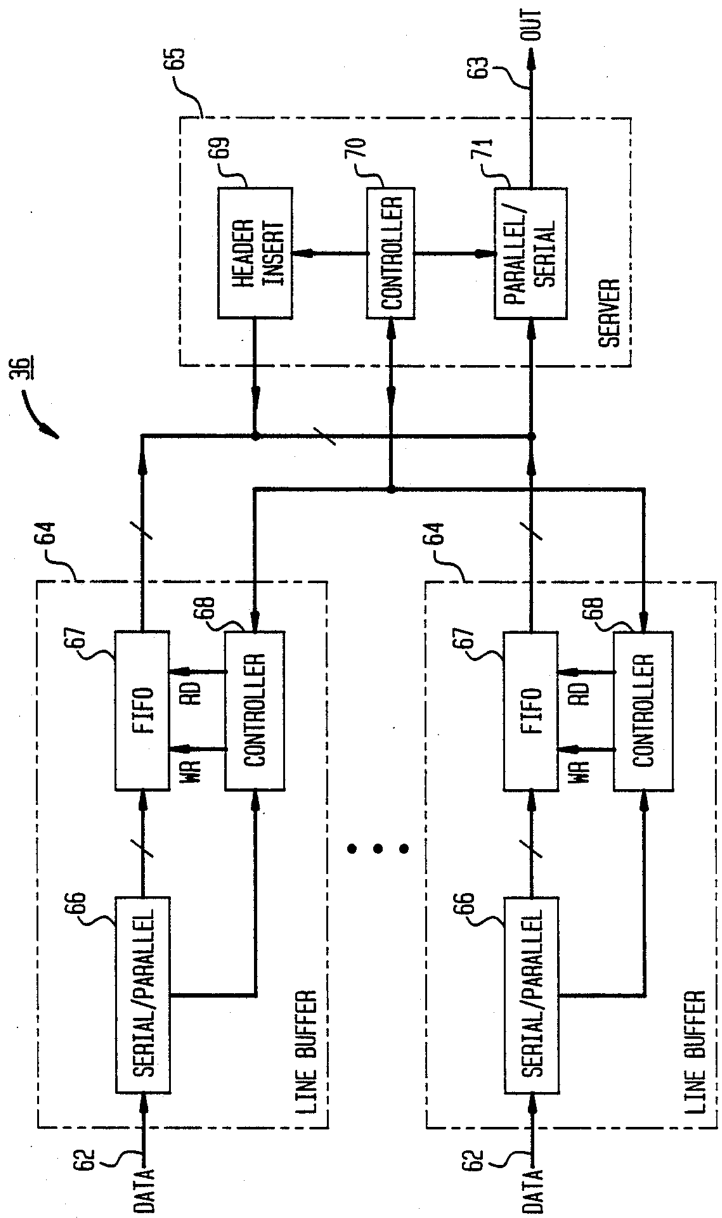
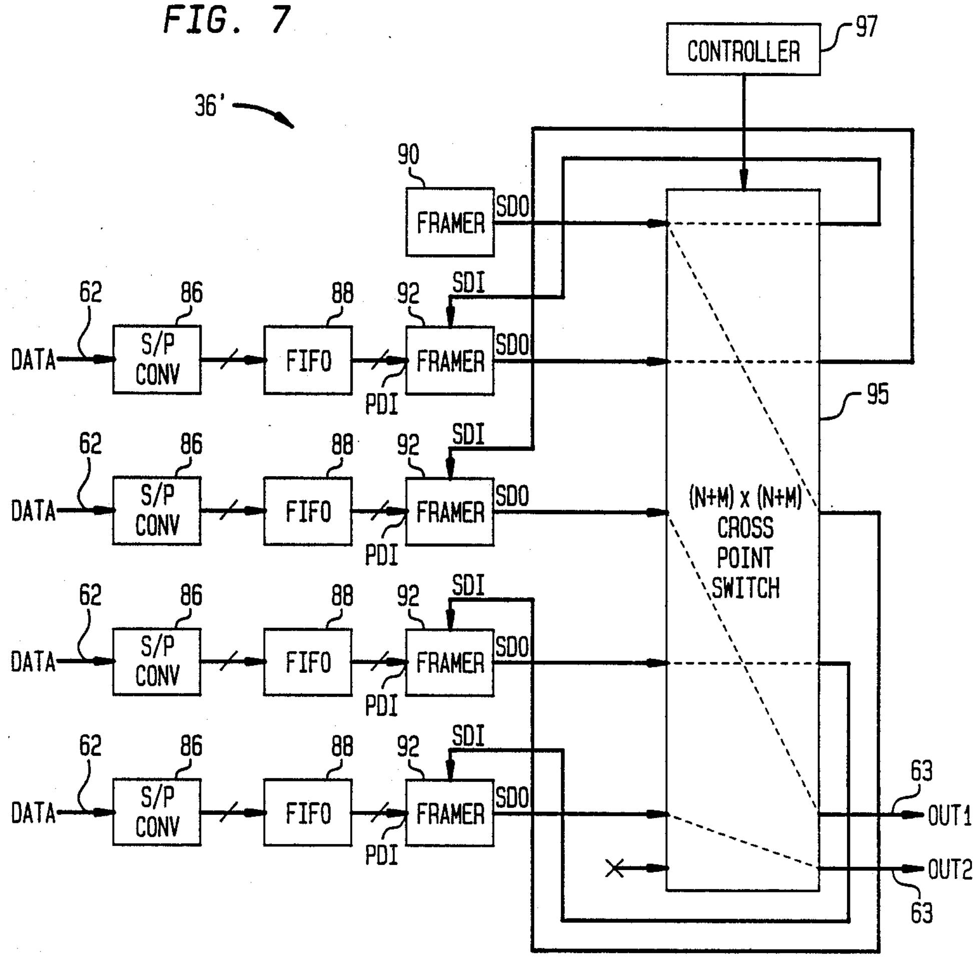
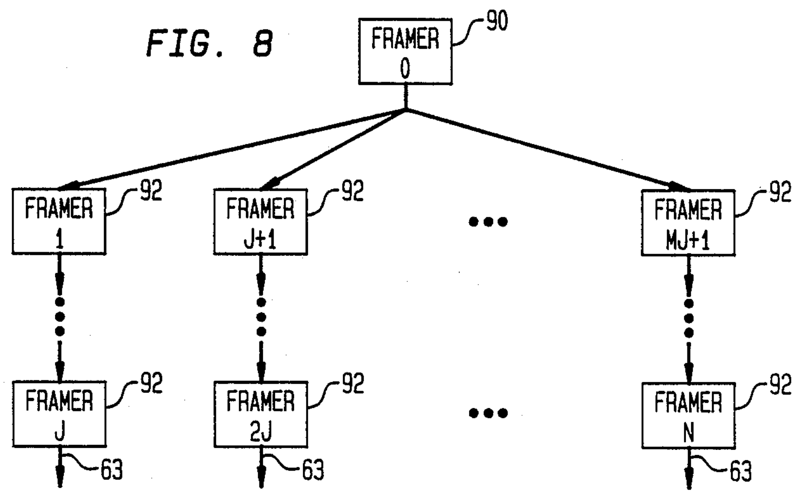

36
65
63
OUT
69
HEADER INSERT
70
CONTROLLER
71
PARALLEL/ SERIAL
SERVER
64
67
FIFO
68
RD
WR
CONTROLLER
66
SERIAL/PARALLEL
LINE BUFFER
62
DATA
64
67
FIFO
68
RD
WR
CONTROLLER
66
SERIAL/PARALLEL
LINE BUFFER
62
DATA

FIG. 7



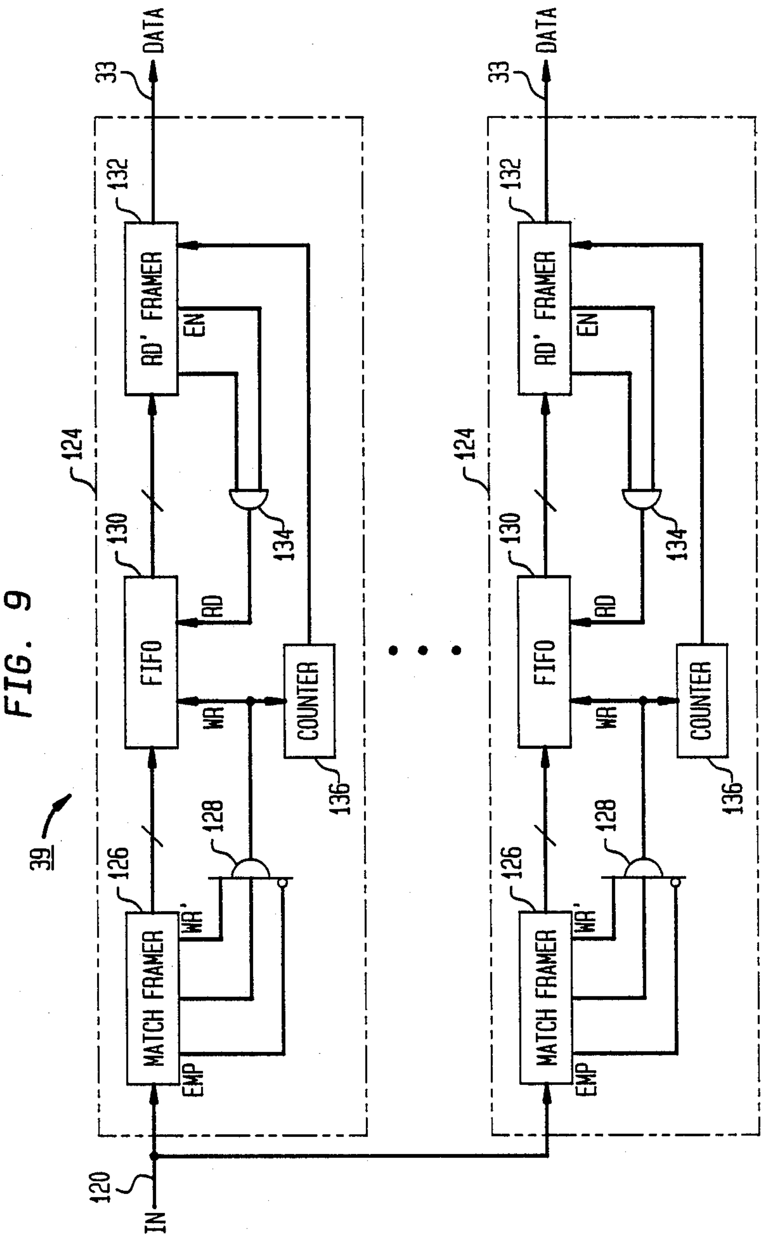
36'
CONTROLLER
97
90
FRAMER
SDO
SDI
62
86
88
92
DATA
S/P CONV
FIFO
FRAMER
PDI
95
(N+M) x (N+M) CROSS POINT SWITCH
63
OUT1
OUT2

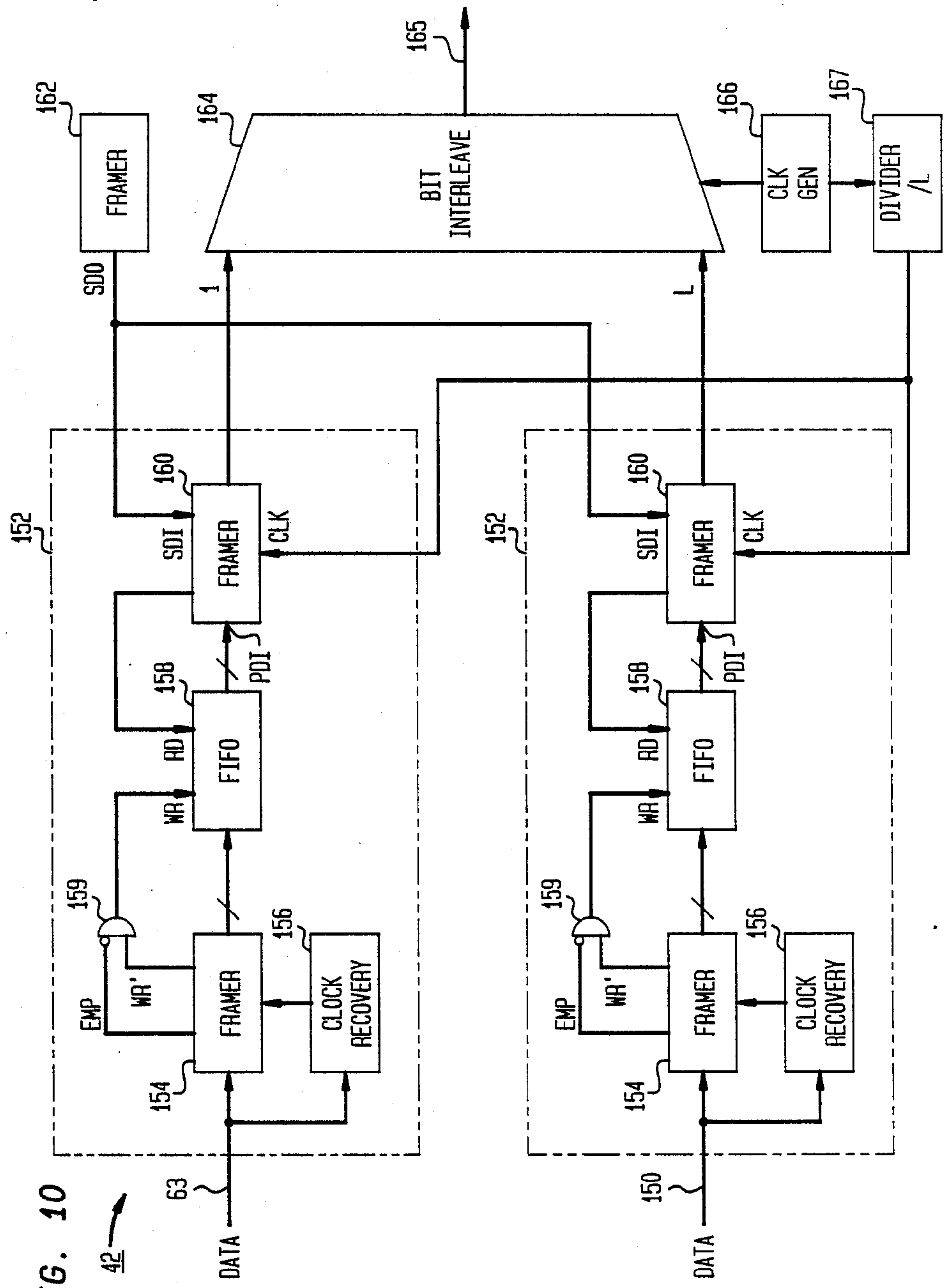
FIG. 8



FRAMER 0
90
FRAMER 1
92
FRAMER J+1
FRAMER MJ+1
FRAMER J
FRAMER 2J
FRAMER N
63

FIG. 9


39
IN
120
MATCH FRAMER
EMP
WR'
126
128
FIFO
WR
RD
130
COUNTER
136
134
124
RD' FRAMER
EN
132
33
DATA



FRAMER
162
SDO
BIT INTERLEAVE
164
165
1
L
CLK GEN
166
DIVIDER /L
167
152
160
SDI
FRAMER
CLK
158
PDI
RD
FIFO
WR
159
EMP
WR'
FRAMER
154
156
CLOCK RECOVERY
63
150
DATA
42

FIG. 10

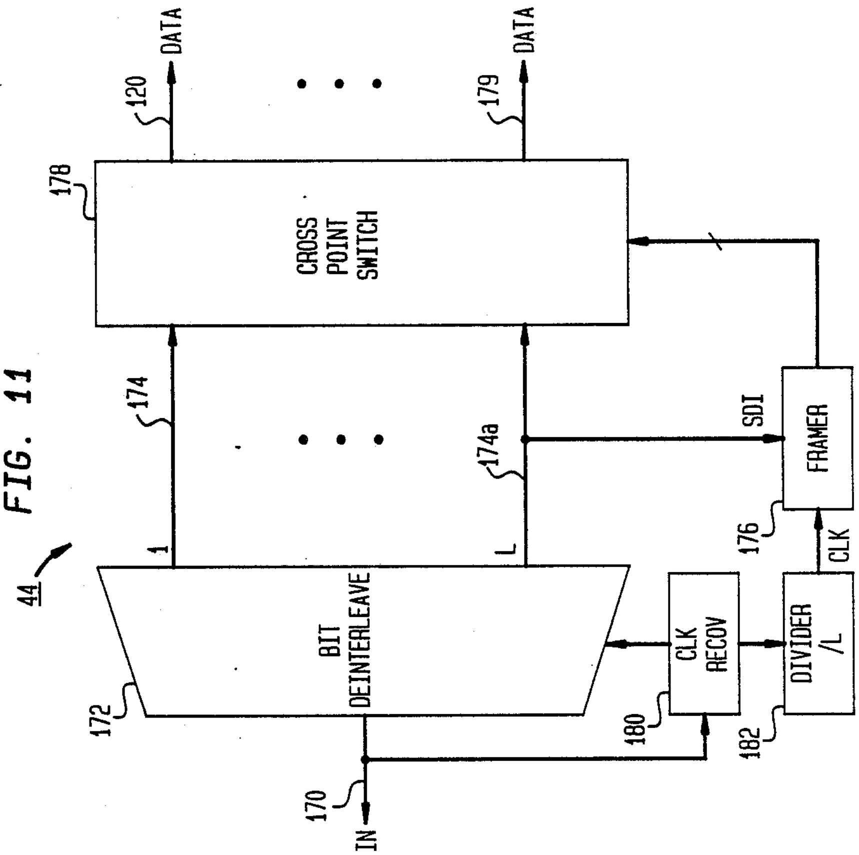
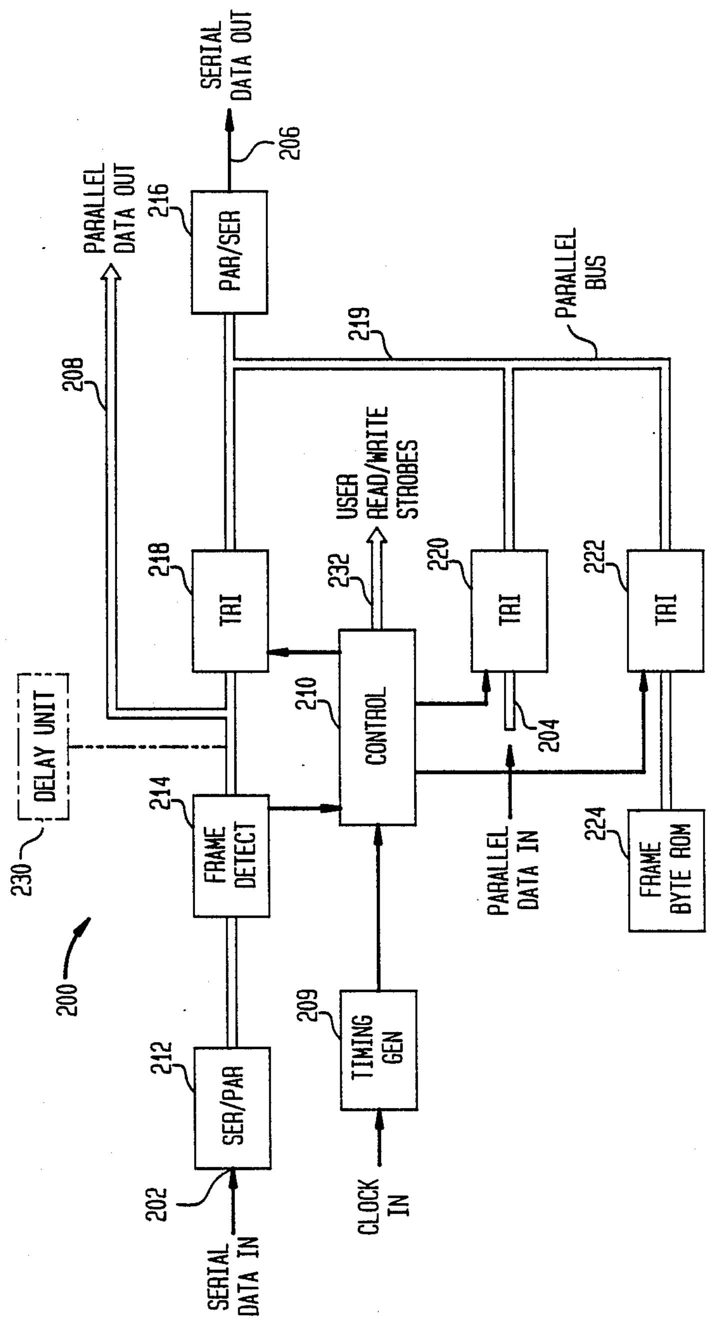

DATA
120
DATA
179
178
CROSS POINT SWITCH
174
174a
SDI
FRAMER
176
CLK
1
L
44
BIT DEINTERLEAVE
CLK RECOV
DIVIDER /L
172
180
182
170
IN

FIG. 11

FIG. 12


SERIAL DATA OUT
206
PARALLEL DATA OUT
216
PAR/SER
208
219
PARALLEL BUS
USER READ/WRITE STROBES
218
TRI
232
220
TRI
222
TRI
210
CONTROL
204
230
DELAY UNIT
214
FRAME DETECT
224
FRAME BYTE ROM
PARALLEL DATA IN
200
212
SER/PAR
209
TIMING GEN
202
SERIAL DATA IN
CLOCK IN

FRAMER CIRCUIT FOR USE IN A DTDM NETWORK

RELATED APPPLICATIONS

The following applications contain subject matter related to the subject matter of the present application, are assigned to the assignee hereof and have been filed on the same date as the present application.

1. H. J. Chao, "DTDM Multiplexer with Cross-Point Switch", having Ser. No. 118,979.
2. M. W. Beckner, F. D. Porter, K. Shu, "DTDM Multiplexing Circuitry", having Ser. No. 118,897.
3. H. J. Chao, S. H. Lee, "Time Division Multiplexer for DTDM Bit Streams", having Ser. No. 118,978.
4. H. J. Chao, S. H. Lee, L. T. Wu, "Dynamic Time Division Multiplexing", having Ser. No. 118,977.

FIELD OF THE INVENTION

The present invention relates to a data transmission technique referred to herein as Dynamic Time Division Multiplexing (DTDM) and a set of multiplexers and demultiplexers required to apply DTDM in an actual telecommunications network. DTDM is capable of effectively handling both circuit and packet traffic and thus provides a migration strategy between the present circuit switched telephone network and the future broadband packet switched network. More particularly, the present invention relates to a circuit known as a framer circuit. This circuit is important for the implementation of specific embodiments of multiplexers and demultiplexers suitable for use in a network utilizing dynamic time division multiplexing.

BACKGROUND OF THE INVENTION

Presently, there are significant uncertainties when it comes to predicting the future demand for broadband telecommunications services such as high definition video and interactive data communications. This uncertainty in the future demand for broadband telecommunications services has a significant impact on the design of public telephone networks. First, to satisfy the unknown growth pattern in future service demands, it is desirable to have a robust network design that can be easily modified in response to changes in demand for particular telecommunications services. Second, the network must be able to handle vastly different types of traffic ranging from low speed data and voice to full motion video. Third, depending on the demand for wideband services, a network design must be capable of providing a migration strategy from existing copper wires and circuit transmission and switching facilities to optical fibers and the succeeding generations of high speed packet transmission and switching facilities, which packet facilities are used in connection with the delivery of wideband telecommunications services. These three criteria determine the selection of the three major components of a network design: network topology, transmission systems and switching systems. Here, the concern is primarily with transmission systems and transmission techniques which meet the foregoing criteria.

Two important types of commercially used transmission systems are circuit systems and packet systems. Typically, circuit systems utilize time division multiplexing (TDM) as a transmission technique. When TDM is used, each data stream comprises frames which are subdivided into slots. Corresponding slots in each

frame are allocated to specific connections. For example, the first slot in each frame is allocated to one specific connection and the second slot in each frame is allocated to a second connection, etc. Each frame also includes a field which contains transmission overhead information including frame synchronization words and control words. This traditional circuit transmission format can be extended to multiple bit rate services by allocating multiple slots in each frame to high bandwidth services. In such circuit transmission systems, a combination of space division switching and time division switching is utilized at the network switches to swap time slots between various bit streams so that connections to and between specific subscribers are established.

Historically, the first digital circuit transmission systems were introduced during the 1960's. These first digital circuit transmission systems were introduced in inter-office trunking applications to carry 24 voice channels by a single 1.544 Mb/sec digital stream. This is known as the **DS-1** signal. Subsequently, the wide deployment of digital channel banks in the public telephone network required the multiplexing of several **DS-1** signals into a higher speed bit stream to efficiently utilize available transmission links. As the network grew further, continuing efforts to effectively multiplex tributaries having different bit rates into a common bit stream resulted in the well-known hierarchical multiplexing plan comprising the **DS-1** (1.544 Mb/sec), **DS-1C** (3.152 Mb/sec), **DS-2** (6.312 Mbit/sec), **DS-3** (44.736 Mb/sec) and **DS4** 274.176 Mb/sec signals.

Conventional circuit transmission systems suffer from a number of shortcomings. Perhaps the most important problem is the multiplexing hierarchy itself. An important result of the hierarchy is an inherent lack of flexibility. Since the network can only transmit the set of signals in the hierarchy, every telecommunications service has to meet the stringent interface requirement of given hierarchical signal bit rates, instead of the particular service being able to transmit at its own natural bit rate. Therefore, the packet mode of transmission which is inherently bit rate flexible is favored for future broadband networks which are to be adapted to deliver enhanced telecommunication services such as high definition video and interactive data communications.

In contrast with circuit transmission systems which transmit data in frames subdivided into slots, packet transmission systems transmit data in discrete blocks or packets, with each packet having an address header at the front thereof. At the network switches, packets are routed from a specific input line to a specific output line, based on address information contained in the packet header. In this way data packets can be routed from a particular subscriber location, through a telecommunications network, to another subscriber location. Packet transmission techniques and especially fast packet transmission techniques (see e.g., R. W. Muise et al., "Experiments in Wideband Packet Technology", Proc 1986 International Zurich Seminar on Digital Communications, pp. 136–138) are inherently bandwidth flexible (i.e. the number of packets generated by a given service per unit time is flexible) and thus are suitable for wideband enhanced communications services. Accordingly, it is desirable to introduce packet transmission technology into the public telephone network, which up to now is based primarily on circuit transmission technology.

The commonly-held view as to how to introduce packet technology into the public network is to deploy a packet overlay network because the existing network is optimized for circuit transmission and is therefore incompatible with packet transmission techniques. Accordingly, many deployment strategies recommend constructing an overlay packet network for a set of wideband services and hope that the migration of new services to the packet overlay network will allow the existing circuit transmission network to be phased out slowly. The main advantage of a packet overlay network is the quick realization of an end-to-end network for new services. However, the approach requires a large initial capital investment and increases operational cost by requiring the management of multiple separate networks.

As described in the above noted related applications, it is desired to provide an alternate approach for introducing packet transmission technology the public telephone network, which approach requires the replacement of existing transmission components but not the implementation of an entirely new network. Thus, is desired to provide a digital data transmission system capable of handling both existing hierarchical circuit traffic and packet traffic.

It should be noted that recent advances in network switch designs have blurred the distinction between packet networks and circuit networks. A typical switch for use in a telecommunications network has three major components: control processor, switch interfaces, and interconnection network. The control processor handles call set-up and tear-down, maintenance and administrative functions. The switch interfaces convert transmission formats (i.e., the format data has when transmitted between switching nodes) to switch formats (i.e., the format data has when processed within switching nodes). The interconnection network routes information blocks from specific input lines to specific output lines of the switch. For the existing digital circuit systems used in the public telephone network, the information in a specific time slot on an incoming line is transferred, via the switch, to a specific time slot on an outgoing line. Thus, the interconnection network serves as a cross-connect for the incoming signals on a slot-by-slot basis.

It has recently been shown (see e.g., Day-Giacopelli-Huang-Wu U.S. patent application Ser. No. 021,664 entitled Time Division Circuit Switch, filed on Mar. 4, 1987 and assigned to the assignee hereof now U.S. Pat. No. 4,782,478, issued Nov. 1, 1988) switch for use in a circuit network can be built using a self- routing packet interconnection network. An example of such a self-routing packet network is the Batcher-banyan network. Based on the address headers associated with fixed sized packets, the Batcher-banyan network routes a plurality of packets in parallel to specific destination addresses (i.e., specific output lines) without internal collisions. Thus, to mimic the operation of the conventional time-space-time switches used in circuit networks, switch interfaces are provided which perform the time slot interchange function and which are able to insert headers in front of circuit slots to convert such slots into packets for routing through the self-routing interconnection network and able to remove headers from packets leaving the self-routing interconnection network to reconvert packets back into conventional circuit time-slot format.

In addition to circuit and packet transmission, another mode of digital transmission is known as Asynchronous Time Division Multiplexing (ATDM). See e.g., W. W. Chu "A Study of Asynchronous Time Division Multiplexing for Time Sharing Computer Systems" Proc AFIPS Vol 35, pp. 669–678, 1969 and A. Thomas et al. "Asynchronous Time Division Techniques: An Experimental Packet Network Integrating Video Communication" Proc International Switching Symposium, May 1984. ATDM is used in connection with continuous and bursty data traffic. ATDM uses channel identifiers with actual data to allow on-demand multiplexing of data from subscriber terminals with low channel utilization. The channel identifiers and associated data form time slots. However, ATDM is bit rate flexible since the appearance of packets can be asynchronous. Slot timing is obtained from a special synchronization pattern which is inserted into unused time slots. Since the synchronization pattern appears only in unused time slots, ATDM cannot be used to carry existing high speed hierarchical signals wherein the loading is close to one hundred percent.

In short, the situation is that the present public telephone network utilizes circuit transmission technology and the associated time division multiplexing transmission techniques, while future broadband services, the demand for which is presently uncertain, are best offered using packet transmission technology. It is therefore an object of the invention to provide a transmission system which is capable of integrating present circuit traffic with future packet traffic so as to provide a flexible migration strategy from the existing copper wire based circuit network to succeeding generations of high bandwidth packet transmission networks. It is a further object of the invention to provide a circuit known as a framer circuit, which circuit is important for the implementation of specific multiplexers and demultiplexers suitable for use in a network utilizing the inventive transmission systems.

SUMMARY OF THE INVENTION

The digital network transport system, referred to herein as Dynamic Time Division Multiplexing (DTDM), is a flexible network transport system capable of effectively handling both circuit and packet traffic. By combining conventional time division multiplexing techniques and packet transmission techniques, DTDM enables a flexible transition from the existing circuit type networks to future broadband packet transmission networks.

In a network utilizing DTDM, each transmission bit stream is divided into frames. These frames are the fundamental unit of data transport in DTDM. Each such frame comprises two fixed length fields: overhead and payload. The overhead field includes, for example, a frame alignment word for frame timing and the empty/full status of the frame. The payload field of each frame may be filled with a data packet including header or a slot from a circuit transmission stream. Before a slot from a circuit transmission stream can be inserted into the payload field of a DTDM frame, it must first be converted into a packet-like form with a header at its front. Viewed another way, each occupied DTDM frame comprises a transmission overhead field, a header field, and a data field. Thus, the DTDM transmission format is a combination of the circuit transmission format and the packet transmission format.

In the DTDM system, packet and circuit traffic can be multiplexed through the same multiplexer. Thus, such a multiplexer can have continuous circuit type tributaries and bursty packet tributaries. To multiplex such diverse traffic, a train of DTDM frames with empty payload fields is generated. This train has a bit rate which defines a basic backbone transmission rate for the DTDM transmission system. Data in the form of packets or circuit slots with headers attached are inserted into the empty frames to form the DTDM bit stream.

An appropriate analogy is as follows. The stream of empty DTDM frames may be analogized to a train of empty freight cars. The empty freight cars are then filled with data from the various tributaries which may have been in circuit or packet format.

Illustratively, a DTDM multiplexer may be used to merge traffic from three different communications sources or tributaries into a single DTDM bit stream. These tributaries may be a digital phone generating 64 Kilobits/sec PCM voice, a graphics terminal sending bursty data at 1 Megabit/sec, and a circuit transmission stream operating at the DS3 rate of about 45 Megabits/-sec. Illustratively, the bit rate of the backbone DTDM bit stream is 150 Megabits which yields 144,000 frames per second given a 130-byte frame size. The available frames are shared by the three tributaries by giving higher priority to the circuit tributary, and allowing the voice and graphics tributaries to contend on a first-come, first-served basis. The circuit tributary seizes one out of every three empty frames passing by. Thus the regularity of the circuit transmission will be maintained throughout the DTDM transmission link. Illustratively, the voice source is packetized by accumulating up to 15 milliseconds worth of voice samples before inserting this information into an empty DTDM frame along with a header. In this case the voice tributary will on average seize one out of every 2,160 frames. Similarly, at a rate of 1 Megabit per second, the graphics tributary will fill one frame out of 150. In this way, three diverse data streams are multiplexed into a single bit stream.

As a second example, DTDM can be used as a replacement transmission technology to carry existing inter-office traffic. More specifically, consider the need to multiplex and transmit three hierarchical signals at the DS1, DS2, and DS3 rates, respectively, for point-to-point transmission between two offices. The traditional TDM approach would utilize a step-by-step heriarchical approach to multiplex and to subsequently demultiplex these signals. The conventional hierarchical multiplexing scheme requires line conditioning and synchronization circuitry at each level of the hierarchy as well as hardware for bit interleaving.

In contrast, using a DTDM multiplexer, time slots from each of the three signals would be inserted into the empty frames in a basic DTDM backbone signal. If the backbone signal is 150 megabits per second and comprises 144,000 frames per second, the DS3 signal would require one out of every three DTDM frames, the DS2 signal would require approximately one out of every twenty-one DTDM frames and the DS1 signal would require approximately one out of every eighty-four of the empty DTDM frames.

In an actual network, the above-described DTDM streams at the basic backbone bit rate generally contain empty frames; thus DTDM streams may be multiplexed into more densely populated DTDM bit streams at the same bit rate. These more densely populated basic backbone rate bit streams may then be multiplexed into higher bit rate streams for point-to-point inter-office transmission.

Details of the assemblers needed to form the basic DTDM bit streams, the disassemblers needed to disassemble the basic DTDM bit streams, and the set of multiplexers and demultiplexers needed to implement DTDM in an actual network are described in detail below along with a framer circuit which plays a significant role in particular implementations of the assemblers/disassemblers and multiplexers/demultiplexers.

More particularly, the framer circuit performs a number of functions in a DTDM network including generating trains of empty DTDM frames, enabling the writing of data packets into specific DTDM frames and the examination of header data in specific DTDM frames to generate signals for the control of peripheral circuits. The framer circuit may be formed as a single chip.

The framer circuit has a serial data input, a parallel data input, a serial data output and a parallel data output. Timing information for the framer is provided by a timing generator. The framer circuit operates under control of a control unit which illustratively comprises one or more finite state machines.

A data packet may be inserted into an empty DTDM frame in a DTDM bit stream using the framer circuit. The DTDM frame is received at the serial input of the framer circuit and is converted to parallel form using a serial to parallel converter. The frame is then detected by a frame detector circuit. The frame detector circuit is in communication with the control unit and communicates to the control information such as the empty/-full status of the frame.

The data packet to be written into the frame is received at the parallel input of the framer circuit. When an empty frame is received in the framer circuit, the control transmits a signal to a tristate device which enables the data packet to be inserted into the frame before it leaves the framer circuit. Frames leave the framer circuit via a parallel-to-serial converter and the serial data output.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** schematically illustrates the DTDM transmission format;

FIG. **2** schematically illustrates the formation of a backbone DTDM bit stream;

FIG. **3** schematically illustrates an end-to-end network using DTDM;

FIG. **4** illustrates an assembler for combining diverse tributary data streams into a ingle DTDM stream;

FIG. **5** illustrates a disassembler for separating a DTDM bit stream into diverse tributary data streams;

FIG. **6** illustrates a multiplexer for combining a plurality of DTDM bit streams into a single more densely occupied DTM bit stream having the same bit rate;

FIG. **7** illustrates a N:M multiplexer for combining a plurality of DTDM bit streass;

FIG. **8** illustrates how the input lines in the multiplexer of FIG. **7** are grouped;

FIG. **9** illustrates a demultiplexer for separating a densely occupied DTDM bit stream into a plurality of less densely occupied DTDM bit streams;

FIG. **10** illustrates a multiplexer for point-to-point transmission;

FIG. **11** illustrates a demultiplexer for use in connection with point-to-point transmission; and

FIG. 12 illustrates a framer circuit, in accordance with an illustrative embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

1. DTDM Transmission Format

DTDM is an approach to data transport which can handle both TDM hierarchical signals and packet traffic in a common integrated structure, while allowing complete bit rate flexibility. As illustrated in FIG. 1, the transmission bit stream is divided into frames 1. The DTDM frame is the fundamental unit of information transport in the DTDM transmission scheme. The frames come one after the other so as to form a continuous chain or train.

Each frame 1 comprises two fixed length fields designated transmission overhead (T) and payload in FIG. 1. Illustratively, each frame comprises 130 bytes with 10 bytes being allocated to the transmission overhead field. Typically, the bit rate of the DTDM bit stream illustrated in FIG. 1 is about 150 Megabits/sec. The following information may be available in the overhead field of every DTDM frame; frame alignment word for frame timing, empty/full status of the frame, and span identification.

As shown in FIG. 1, the payload field of each frame may be filled with a data packet including a header (H) or a slot from a circuit transmission stream. However, before a slot from a circuit transmission stream can be inserted into the payload field of a DTDM frame, it must first be converted to packet-like form by the insertion of a header (H) at its front. Viewed another way, each occupied DTDM frame comprises a transmission overhead field, a header field, and an information field. Thus, the DTDM transmission format is a combination of the circuit transmission format and the packet transmission format. The packet header provides information such as channel number, line number, error detection, etc. In general, only the information required in every frame gets permanent bandwidth allocation in the transmission overhead field.

FIG. 2 schematically illustrates the formation of a DTDM bit stream. The DTDM bit stream assembler 3 can combine into a single bit stream both continuous circuit tributaries and bursty packet tributaries. Three such tributaries are illustrated in FIG. 2. They are: a digital phone tributary 5 generating 64 Kilobits/sec PCM voice, a tributary 7 from a graphics terminal sending bursty data at one megabit per second, and a circuit transmission stream 9 operating at the DS3 rate of about 45 Megabits/sec. Each of the three tributaries has a characteristic shading in FIG. 2 so that it is possible to follow how data from the three tributaries is combined to form the DTDM bit stream.

To multiplex such diverse traffic, a train 10 of DTDM frames with empty payload fields is generated. This train 10 has a bit rate which defines a basic backbone transmission rate for the DTDM system. Each of the frames in the train 10 has an occupied transmission overhead field (T).

Illustratively, the train of frames has a bit rate of about 150 Megabits per second and comprises 144 K blocks/sec. The assembler 10 serves to insert data from the tributaries 5, 7, 9 into the payload fields of the DTDM frames in the stream 10. To accomplish this, the tributaries 5, 7, 9 are first packetized using packetizers 11, 13, 15, respectively to form the packetized streams 17, 19, 21. Each packet comprises a header (H) and an information field. In the case of the tributary 5, up to 15 milliseconds of speech samples are accumulated to form a packet. In the case of the circuit tributary each slot is converted to packet form by placing a header at the front thereof.

To form the DTDM stream 10, the packets comprising the streams 17, 19, 21 are inserted into the empty payload fields of the empty frames in the stream 10. The empty frames are shared by the three tributaries by giving higher priority to the circuit tributary 9 and allowing the voice and graphics tributaries 5, 7 to contend for empty frames on a first-come, first-served basis. Thus, the circuit tributary seizes one out of every three frames so that the regularity of the circuit transmission is maintained throughout the DTDM transmission link. Similarly, the voice tributary will seize one out of every 2,160 frames and the graphics tributary will seize on average one out of every 150 frames. It should be noted that the bit stream 12 is not 100% occupied and that some frames remain empty. In this way, three diverse tributaries are multiplexed into a single DTDM bit stream.

2. A Network Utilizinq DTDM

FIG. 3 schematically illustrates an end-to-end network 20 utilizing DTDM. The network 20 connects to customer premises equipment (CPE) 22, of which three types are illustrated, namely video, voice and data.

In the network 20, three multiplexing stages are required to support end-to-end transport. In the user-network interface stage 30, an assembler 32 receives data streams on lines 21 from the customer premises equipment 22 and combines these streams into a basic backbone DTDM stream of the type discussed in connection with FIGS. 1 and 2. Similarly, disassembler 34 tears apart a basic DTDM bit stream arriving on line 33 and distributes the data to the appropriate customer premises equipment 22 via lines 23.

As indicated above, the DTDM bit stream formed by the assembler 32 is not 100% occupied. Thus the multiplexer 36 in the remote electronics stage 38 is used to combine several DTDM bit streams arriving on lines 62 into a more densely occupied DTDM bit stream of the same bit rate to achieve greater transmission efficiency. Similarly, the demultiplexer 39 separates a densely populated DTDM bit stream arriving on line 120 into less densely populated DTDM bit streams transmitted via lines 33, so that the data contained therein can ultimately be routed to the correct customer premises equipment.

In the point-to-point stage 40, a plurality of DTDM bit streams arriving via lines 63, 150 are time division multiplexed by means of time division multiplexer 42 for high speed point-to-point transmission via line 165 to a network switch (not shown). For example, the multiplexer 42 receives one DTDM stream via a line 63 from multiplexer 36 and another DTDM stream via line 150. The DTDM bit stream transmitted via line 150 is formed by DTDM assembler 43 and contains the data of three DS3 tributaries 45.

Time division demultiplexer 44 receives a high speed bit stream from a switch (not shown) via line 170 and demultiplexes this stream into a plurality of DTDM streams. One DTDM stream containing data for customer premises equipment goes to demultiplexer 39 via line 120 and another DTDM stream comprising DS3 slots goes to disassembler 45 via line 179.

3. DTDM Assembler and Disassembler

The function of the DTDM bit stream assembler **32** of FIG. **3** is to packetize each incoming data stream associated with one particular customer service or transmission channel and then embed these packets into the basic DTDM transmission frames. The assembler **32** is shown in greater detail in FIG. **4**.

The assembler **32** comprises a plurality of interface units **50**. Each interface unit **50** serves to interface an associated data input **21** with the DTDM bit stream. A DTDM bit stream comprising empty frames with empty payload fields is generated by framer unit **52**. A detailed description of the framer unit is provided below.

Each interface unit includes a framer unit **53**. The framer units **52, 53** are connected together in a daisy chain fashion. The frames comprising the DTDM bit stream are passed along the daisy chain from one framer unit to the next. More particularly, the DTDM bit stream leaves the serial data output (sdo) of the framer unit **52** and enters the serial data input (sdi) of the topmost framer unit **53**. The DTDM bit stream leaves the topmost framer **53** via its serial data output (sdo). The DTDM bit stream then enters the serial data input (sdi) of each succeeding framer unit and leaves via the serial data output (sdo) of each framer unit. The DTDM bit stream leaves the serial data output of the lowermost framer via line **62**. As shown in FIG. **3**, line **62** serves to transmit the DTDM bit stream to the DTDM multiplexer **36**. If the DTDM frame currently located at the framer unit **53** of a particular interface **50** is empty, that interface may insert a packet into the payload field of the DTDM frame.

The data inputs **21** to the assembler **32** are connected to the customer premises equipment **22** of FIG. **3** and may have a wide range of bit rates; for example, the data inputs **21** can be video, voice, data, or different digital hierarchical transmission signals (DS-**1**, DS-**2** and DS-**3**). Therefore, the assembler architecture must be capable of efficiently accommodating different input bit rates and be flexible enough to allow for future expansion or for the changing of particular input connections to different services. The architecture shown in FIG. **3** provides the capability to easily add or drop a particular input service.

Each input **21** is connected to a packetizer **55** which forms part of the associated interface unit **50**. The packetizer **55** puts the incoming data into a packet structure by adding a packet header at the beginning of appropriate segments of the input bit stream. The packet header carries information about the packet, such as packet occupancy, channel identification number, line identification number, check sum and so on. Illustratively, the channel identification number is used to identify the input service from which the packet originated. After the data is put into a packet structure, it is stored in a FIFO **57** with byte wide format. The framer unit **53** then reads the data from the FIFO **57** into its parallel data input (pdi) **58** and generates properly framed data bits which are inserted into an empty payload field of a DTDM frame currently at the particular framer unit **53**.

However, a framer unit **53** will not read the data from the FIFO **57** unless two conditions are met. One is that the "packet-ready" pulse signal from the packetizer **55** is asserted, indicating one packet is completely stored in the FIFO. The other condition is that the incoming DTDM frame on the serial data input (sdi) of the framer **53** is not already occupied by a valid packet, i.e. the incoming DTDM frame is empty. Thus, an empty or "emp" signal is transmitted from the framer **53**. The "packet-ready" signal triggers an enable signal, "en", in the framer unit to be asserted for the whole frame transmission period allowing the data packet to be moved from the FIFO **57** through the framer **53** and into the DTDM bit stream. Using the "emp" and "en" signals, control logic **59** controls the reading of a packet out of the FIFO **57** and into the framer **53**.

Since the framer units **53** are daisy-chained together, the contention for empty DTDM frames is automatically resolved in favor of input services having positions closer to the empty frame generator.

In order to simplify the assembler **32** of FIGS. **3** and **4** and hence reduce the building cost, one practical assumption may be utilized; the total traffic of all inputs at any given time is less than the bit rate of the basic backbone DTDM stream.

The topmost framer **52** in FIG. **4** does not have any input service connected to it. It generates the chain of empty DTDM frames which are sent to the following framers **53**. If none of the interfaces **50** insert a packet into a particular frame, an empty frame is finally sent out through the serial data output (sdo) of the bottommost framer unit on lead **62**.

After the DTDM bit stream has traveled through the entire communications network **20** of FIG. **3**, which network includes multiplexers, switches, and demultiplexers, etc., the DTDM bit stream is disassembled and the data distributed to the appropriate customer services equipment. In the network **20** of FIG. **3**, the disassembler **34** is used for this purpose. The disassembler **34** is shown in greater detail in FIG. **5**. Illustratively, the disassembler **34** removes both the transmission overhead and packet header field from each incoming DTDM frame and distributes the data contained in the frame to the desired customer premises device.

More particularly, the assembler **34** comprises a plurality of interfaces **66**. Each interface **66** receives the incoming DTDM bit stream via line **33** (see FIG. **3**) and is illustratively connected to one customer premises device via an output lines **23** (see FIG. **3**). Each incoming DTDM frame is simultaneously received by the framer unit **70** in each interface **66**. However, only packets containing data to be transmitted to the associated customer premises equipment are transferred from the framer **70** to the associated FIFO **72**. To accomplish this, the packet occupancy and channel identification number are examined by the framer **70**. The framer **70** in turn generates proper control signals via lines **73**, which, along with control logic **74**, determine whether or not the packet carried in the payload field of the particular DTDM frame will be written into the FIFO **72** of the particular interface unit so that the data contained in the packet can be transmitted to the associated customer premises equipment.

Recovering the correct frequency from the incoming data is a very challenging task. Although for each kind of customer premises equipment or service the frequency is known, the difference between the local reading clock used to read data out of the FIFO **72** and the clock which was used to load data into empty frames at the transmit end may result in overflow or underflow of the FIFO **72**. Illustratively, a phase locked loop **78** is used to modify the local reading clock in order to cancel this difference in clock rates.

As shown in FIG. 5, the local reading clock signal (line 73a) used to read data out of the FIFO 72 is phase locked with the incoming data so that the data can be read out correctly from the FIFO 72 without overreading or underreading. The rate at which data is read out of the FIFO is determined by the frequency of the voltage controlled oscillator 76 in the phase locked loop 78.

The packet is written into the FIFO 72 with the network clock rate, but read out at a rate dependent on the particular equipment to which the data is transmitted. An "hf" signal which indicates that the FIFO 72 is half full is smoothed out by a low-pass filter 75 whose output is used to control the output frequency of a voltage-controlled oscillator 76. If information is read out of the FIFO 72 faster than information is written into the FIFO 72, then the 'h' signal will not be asserted. This causes the voltage output from the low-pass filter 75 to decrease, reducing the output frequency produced by the voltage controlled oscillator and reducing the rate at which data is read out of the FIFO 72. Similarly, if information is read out of the FIFO more slowly than it is being written into the FIFO 72, the "hf" signal will be asserted and the voltage controlled oscillator frequency will be increased so that the read clock signal frequency is larger. The same interface unit 66 can be used for different customer premises devices by choosing a proper frequency for oscillator 69.

Data packet read out of the FIFO units 72 are depacketized by means of depacketizer circuits 79 which serve to remove the headers. The resulting data is then transmitted via lines 23 to the appropriate customer premises equipment.

4. DTDM Bit Stream Multiplexer and Demultiplexer

The function of the DTDM bit stream multiplexer 36 of FIG. 3 is to concentrate a plurality of relatively sparsely occupied incoming DTDM streams into at least one more densely occupied DTDM stream of the same bit rate, resulting in more efficient use of the transmission facility. There is more than one architecture for implementing the DTDM multiplexer 36 of FIG. 3.

One embodiment of such a DTDM bit stream multiplexer is illustrated in FIG. 6. The DTDM multiplexer 36 of FIG. 6 comprises N input lines 62 (see FIG. 3) and one output line 63 (see FIG. 3). Line buffers 64 recognize and queue incoming DTDM frames. The server 65 looks for newly arrived DTDM frames in the line buffers 64, adds a proper line number in the header field, and sends the frames out in a more densely occupied DTDM bit stream.

The primary functions of the line buffers 64 are recognition and queuing of incoming DTDM frames. Each line buffer contains a serial/parallel converter 66 for converting incoming serial DTDM frames into parallel form and a first-in, first-out buffer 67 with capacity for multiple frames. A timing and control circuit 68 operates the line buffer and interfaces it with the server.

The main functions of the server 65 are to look for newly arrived DTDM frames in the line buffers, to modify the header field to include a line number, and to place the DTDM frame in a more densely occupied DTDM bit stream. The server comprises a header insert circuit 69 for modifying the header field of the DTDM frames, a controller circuit 70 for interfacing with the line buffers 64, and a parallel to serial converter 70. The operations of the server are pipelined; while the server reads a DTDM frame from a line buffer and places it in an outgoing DTDM stream, it continues searching line

buffers for DTDM frames. It should be noted that the multiplexer of FIG. 6 is useful for multiplexing packets in non-DTDM transmission formats in addition to being useful for DTDM bit streams.

Another possible architecture for a multiplexer capable of combining several relatively sparsely occupied DTDM bit streams into a more densely occupied DTDM bit stream of the same bit rate builds on the architecture of the DTDM bit stream assembler 32 of FIG. 4. Each input to an interface unit 50 of FIG. 4 is replaced by a serial data link on which a DTDM bit stream arrives. The data packets contained in the frames comprising the incoming DTDM bit stream contend for output frames in an outgoing DTDM bit stream. The frames comprising the outgoing DTDM bit streams are generated by the framer 52 and passed along the chain of interconnected framers 53. The interface units 50 insert data packets from incoming DTDM frames into the frames of the outgoing bit stream to form a more densely occupied DTDM bit stream. The contention for output frames is resolved automatically by the daisy-chained connection of the framer units. Note that no packetizer is needed in the interface units, and the length of each FIFO is preferably more than two frames to prevent data packets contained in incoming frames from being lost.

FIG. 7 schematically illustrates an alternative DTDM bit stream multiplexer for combining a plurality of relatively sparsely occupied DTDM bit streams into a smaller number of more densely populated DTDM bit streams of the same bit rate. The multiplexer 36′ of FIG. 7 has the flexibility to receive N input DTDM bit streams and to transmit M output DTDM bit streams, which allows M output lines to be shared by N input lines. It is known that both the probability of buffer overflow and the average delay for bursty traffic can be significantly decreased by increasing the number of outputs.

Using the multiplexer architecture 36 shown in FIG. 6, it is difficult to build an N:M multiplexer, because the service order is determined by a single central server. However, it is possible to provide a multiplexer system comprising M separate multiplexers of the type shown in FIG. 6, each having N/M input lines and line buffers and one server and associated output line. In contrast, the service order in the multiplexer 36′, of FIG. 7 is determined locally, which results in the flexibility of reassigning input lines to different output lines based on the input traffic statistics.

The N:M multiplexer 36′ of FIG. 7 comprises a plurality of input lines 62 (see FIG. 3) and a smaller number of output lines 63 (see FIG. 3). DTDM frames arriving on the input lines 62 are converted into a byte wide stream by means of the serial-to-parallel converters 86 and stored in the associated buffers (FIFOs) 88. The operation of the framer units 90, 92 is similar to those in the DTDM bit stream assembler of FIG. 3. Each framer 90, 92 has a parallel data input (pdi), a serial data input (sdi) and a serial data output (sdo). Framer 90, the head-end framer unit, doesn't have any input lines connected to it. In normal operation, it continuously sends out a chain of empty frames. The remaining framers 92 take data comprising occupied DTDM frames in the buffers 88, and insert this data into the empty frames generated by the framer 90, so as to combine a plurality of sparsely occupied DTDM bit streams into a smaller number of more densely populated DTDM bit streams.

The N:M multiplexer **36'** of FIG. **7** comprises an $(N+M)\times(N+M)$ broadcasting cross point switch network **95**. The serial data output (sdo) of each framer **90**, **92** is connected to an input of the switch, and the serial data input (sdi) of each framer **92** is connected to an output of the switch as shown in FIG. **7**. The connections through the switch network are controlled by a dedicated controller **97**.

Illustratively, when the system is initialized, the N input lines **62** are divided into M groups, $(1,2\ldots, J)$, $(J+1, J+2, \ldots, 2J), \ldots, (MJ+1, \ldots, (M+1)J)$, where $J=N \bmod M$. The J input lines in each group are logically connected as shown in FIG. **8**. Each group of input lines is associated with one output line. Thus, all of the DTDM frames arriving at the inputs of one group are merged into a single DTDM bit stream which leaves via the associated output. The topmost framer unit **92** in each group receives empty frames broadcast from the framer **90**. Each frame is then passed through the switch **95** from one framer in the group to the next framer in the group. If a particular FIFO **88** has data comprising a DTDM frame and the associated framer **92** receives an empty frame, the data is inserted into the empty frame. Thus, within each group service priority is ranked in descending order with the higher priorities near the top. Ultimately, M relatively densely occupied DTDM bit streams leave the multiplexer of FIG. **6** via the outputs **63**.

Thus, with the addition of the cross point switch, more than one framer **92** receives empty frames from the framer **90** at the same time. This achieves the N:M multiplexing function automatically and with minimal complexity.

If the input lines are not grouped so as to distribute output traffic evenly, the input lines can be regrouped easily by changing the connections within the switching network **95**. For example, a particular input in the first group of inputs may be assigned to any other group, e.g., the second group of inputs, to spread out traffic evenly. The controller **97** must know the traffic statistics of each input line and follow some algorithm to rearrange the inputs and decide the ordering (priority) within each group.

The DTDM multiplexer of FIG. **7** may route DTDM frames arriving on the same input line to different output lines. For example, n frames arriving on an input line have been sent to output #**1**. But the $(n+1)$th frame may be switched to output #**2** because reconfiguration took place to balance traffic among the output lines. This may cause an out of sequence problem if the $(n+1)$th frame arrives at the receive end before the nth frame does. The cost to reorder the frame sequence at the output end may be high. Illustratively, to avoid this problem, one rule may be followed: the input lines carrying services with high bit rate information, such as video, will not be switched from one input line group to another during the service period. For a low bit rate service, such as voice at 64 Kb/s, even if two consecutive frames containing data are dispatched onto two different output lines, the two frames from such a bursty service will be separated by more than several hundred frame intervals. Hence, it is unlikely for there to be an out of sequence problem in this case.

It should be noted that multiplexer architecture of FIG. **7** may be used to multiplex other types of traffic besides DTDM traffic. For example, streams of data packets may be multiplexed together to form more densely occupied streams.

Turning now to FIG. **9**, the DTDM bit stream demultiplexer **39** of FIG. **3** is illustrated in greater detail. The function of the DTDM bit stream demultiplexer **39** is to separate a relatively densely occupied incoming DTDM bit stream into a plurality of relatively sparsely occupied outgoing DTDM bit streams of the same bit rate so that the user data in the frames can ultimately be transported to the proper customer premises devices.

The demultiplexer **39** of FIG. **9** has one input line **120** (see FIG. **3**) and a plurality of output lines **33** (see FIG. **3**). Each output line **33** is connected to the input line **120** by means of an associated interface **124**. Any incoming DTDM frame is simultaneously received by the framer unit **126** in each interface **124**. The frame occupancy and line identification number of each incoming DTDM frame are examined by the framers **126**. If the frame is not empty and the line number is matched, the packet contained therein will be written into the FIFO **130** under the control of logic **128** and then read out of the FIFO **130** by the framer **132** at the output end of the interface **124** under the control of logic **134**. Otherwise, the packet is simply discarded. In this manner, the data from each incoming frame is routed to the correct output line. A counter **136** in each interface is used to count the number of bytes written into the FIFO **130** and generates a signal when a full packet is stored in the FIFO. This signal will inform the output framer **132** to start reading the packet in the FIFO. The framer **132** will assert the 'en' signal during the reading of the entire packet. The framers **132** generate sequences of DTDM frames. These sequences of frames leave the framers **132** via the serial data outputs and form the outgoing DTDM bit streams on the lines **33**. When data packets are present in the FIFOs **130** they are inserted into the frames generated by the framers **132**. In particular embodiments of the demultiplexer, the functions of the framer units **126**, **132** may be performed by a single framer unit.

5. Time Division MUX/DEMUX for DTDM Bit Stream

After relatively sparse DTEM bit streams are concentrated into more densely populated DTDM bit streams of the same bit rate using for example, the DTDM multiplexer **36** of FIG. **3**, a plurality of such more densely populated bit streams may be time division multiplexed into a higher speed data stream using, for example, the time division multiplexer **42** of FIG. **3**. Such high speed data channels may be used for communications to and from central offices.

Usually, the most challenging work in a time division multiplexing system is to synchronize all incoming bit streams so that they have a common bit rate before they are interleaved into a higher bit rate stream. Typically, the input bit streams have the same nominal center frequency but drift independently a small amount from the center frequency. The conventional way to overcome the asynchronization among the input bit streams is positive bit or byte stuffing. The frequency of the high speed output bit stream is made greater than the product of the nominal center frequency and the number of input tributaries. There is usually a bit or byte position reserved for the occasional stuffing of a dummy bit or byte. Also, there is some control overhead used to indicate if the bit or byte at the stuffing position is valid.

By taking advantage of the fact that the frames comprising each input DTDM bit streams are not **100**% occupied, the frequency of the higher speed output bit

stream can be made exactly equal to the nominal center frequency of the input tributaries times the number of the input tributaries. In the case of a DTDM system, this can be accomplished through the positive and negative stuffing of DTDM frames. Since the frequency of each input tributary signal can be adjusted in the positive or negative direction through the insertion or removal of an empty DTDM frame, it is possible to make the frequency of the high speed multiplexed bit stream exactly an integer multiple of the nominal input tributary frequency.

A time division multiplexer **42** (see FIG. **3**) for multiplexing a plurality of DTDM bit streams is illustrated in FIG. **10**. Each input **63, 150** (see FIG. **3**) is connected to an interface unit **152**. Each interface unit **152** comprises a framer **154** which is clocked by a clock signal derived from a clock recovery circuit **156**. The derived clock, which is the actual frequency of the tributary, may differ slightly from the nominal tributary frequency as discussed above. This difference between the nominal and actual frequencies is eliminated in the interface unit. Each incoming DTDM frame will be examined by the framer **154** in the associated interface **152** for its occupancy. The data packets contained in the occupied frames will be written into the FIFO **158** under the control of logic **159** and read out later by the framer **160** at the output end of the interface unit **152**. Empty frames are discarded.

The reading of the data packets from the FIFOs **158** to the parallel data inputs (pdi's) of the framers **160** is synchronized. The serial data input (sdi) of each framer **160** is connected to the serial data output of a framer **162**. The framer **162** serves to broadcast empty frames to the framers **160** so that each framer **160** receives a synchronous chain of empty frames at the nominal tributary frequency. The empty frames received by each framer unit **160** are filled with data packets from the associated FIFO **158** to produce synchronized tributary bit streams at the nominal tributary frequency.

If the actual frequency of a particular tributary is less than the nominal center frequency then on occasion, the associated FIFO **158** will not have a packet to insert into an empty DTDM FRAME. The net effect is that an empty DTDM frame is added so that the tributary acquires a frequency equal to the nominal frequency. However, if the actual frequency of the tributary is larger than the nominal center frequency the net effect is that empty DTDM frames are dropped so that the tributary acquires a frequency equal to the nominal frequency. Illustratively, the difference between the actual and nominal tributary frequencies is on the order of ten parts per million. In this case, a two frame capacity FIFO **158** is sufficient as long as each input tributary has one empty frame in 10/u5/d.

All of the framers **160** send out frames at the same time, with frame alignment being automatically achieved. The aligned frames are then bit interleaved using bit interleaving circuit **164** to produce a single high bit rate bit stream at output **165** (see FIG. **3**). Note that the clocks of the framers **160** are connected together so that data bits coming from the framers **160** are phase aligned and can be bit interleaved directly. The clock for the framers **160** is provided by the clock generator **166** and frequency divider **167**. In an alternative embodiment of a time division multiplexer, instead of bit interleaving, frame or byte interleaving may also be used. If the frame interleaving is used then the multiplexed output bitstream has the same DTDM frame structure, thereby allowing the flexible single transport architecture to grow as the technology advances.

A time division demultiplexer **44** (see FIG. **3**) for demultiplexing the high speed bit stream is illustrated in FIG. **11**. The high speed data stream arrives on input line **170** (see FIG. **3**) and is bit deinterleaved by means of bit deinterleave circuitry **172** into several lower speed tributary bit streams which are transmitted outward on lines **174**. In order to dispatch the bits to correct tributaries, a predetermined span identification (SP ID) is inserted for each tributary before they are multiplexed at the transmit side. The tributary present on line ***174a*** is connected to a framer unit **176**, which will detect the frame boundary and determine by examining the span identification whether or not the bit deinterleave circuitry has correctly aligned the incoming bit stream so that appropriate data goes to appropriate output tributaries. If not, either a skip pulse is generated to rotate the bit sequence or a signal is genererted by the framer **176** and sent to a cross point switch **178** to reassign the order of the bit stream. The bit streams with correct bit assignments appear at outputs **120, 179** (see FIG. **3**). Alternatively, instead of the crosspoint switch **178**, a barrel shifter may be used. It should be noted that the clock for the bit deinterleave circuit **171** and framer **176** is provided by clock recovery circuit **180** and frequency divider **182**. Demultiplexers which operate according to similar principles are disclosed in R. J. Boehm et al. "Standardized Fiber Optic Transmission Systems—A Synchronous Optical Network View" IEEE Journal on Selected Areas in Communications VOL SAC-4 No. 9 pp. 1424–1431 December 1986 and L. R. Linnell "A Wide-band Local Access System using Emerging-technology Components" IEEE Journal on Selected Areas in Communications VOL SAC-4 No. 4 pp. 612–618 July 1986.

6. The Framer Circuit

The framer unit is an important component for the implementation of specific embodiments of the assemblers, disassemblers, multiplexers and demultiplexers which comprise the DTDM network discussed above.

The framer unit performs a number of functions in the DTDM network, including generating trains of empty DTDM frames, enabling the writing of data packets into specific DTDM frames, and the examination of header data in specific DTDM frames to generate signals for the control of peripheral circuits (e.g. in a DTDM demultiplexer to determine if data in a particular DTDM frame belongs to particular customer premises equipment or a particular less densely occupied DTDM bit stream). All of these functions may be carried out by the framer unit discussed below.

A framer unit **200** is schematically illustrated in FIG. **12**. Illustratively, the framer unit **200** is formed as a single chip. The framer unit **200** has a serial data input **202**, a parallel data input **204**, a serial data output **206** and a parallel data output **208**. Timing information for the framer unit **200** is provided by timing generator **209**. The framer **200** operates under control of a control unit **210** which illustratively comprises one or more finite state machines.

As indicated above, a plurality of framer units may be connected in a daisy chain fashion and DTDM frames may be passed from one framer to the next (see e.g., framers **53** of FIG. **4**). Data may be written into an empty DTDM frame as follows. A DTDM frame is received at the serial input **202**. The DTDM frame is

converted to parallel form by serial-to-parallel converter **212** and is detected by frame detector **214**. The frame detector **214** is in communication with the control **210** and illustratively communicates to the control **210** information such as whether or not the frame is empty. Illustratively, the DTDM frame leaves the framer unit via the serial output **206** after conversion to serial form by way of parallel- to-serial converter **216**. However the frame cannot reach the parallel-to-serial converter **216** unless the control **210** applies a signal to the tristate device **218**.

The data to be written into the frame is received at the parallel data input **204** (illustratively from a FIFO **57** in the DTDM bit stream assembler **32** of FIG. **4**). If the particular DTDM frame is empty and data is available at the parallel input **204**, a signal is applied by the control **210** to the tristate device **220** to enable the data to be inserted into the particular DTDM frame via bus **219** before it leaves the framer unit. However, if the DTDM frame is already full the control does not provide such a signal to the tristate **220**. In particular framer units additional information such as span identification may be inserted into specific DTDM frames by means of an additional tristate unit not shown.

The framer unit **200** may also be utilized to generate a chain of empty DTDM packets (see e.g., framer **52** in FIG. **4**). In this case the serial input **202** and associated serial-to-parallel converter **212** are not utilized. Instead, the control **210** applies a periodic signal to tristate **222** so that a frame alignment word is periodically read from frame byte ROM **224** and transmitted via bus **219** to parallel-to-serial converter **216** and serial output **206** so as to define a train of empty DTDM frames. Other information comprising the transmission overhead (T) field of the DTDM frame may also be stored in ROM **224** or provided by other sources connected to the bus **219** via a tristate device operative under the control of the control unit **219**.

In particular situations (see e.g., framers **70** of FIG. **5** and **126** of FIG. **9**), a framer unit receives occupied DTDM frames and the header (H) or transmission overhead (T) fields have to be examined to control peripheral circuit operations such as the reading of data into a FIFO. In this case, a multiple byte delay unit **230** may be included in the path between the serial input **202** and the parallel and serial outputs **208**, **206**. Typically a frame arrives at the serial input **202** and is converted to parallel form by the serial-to-parallel converter **212**. The frame detector detects the frame and supplies necessary information from the header or transmission overhead fields to the control unit **210** which issues appropriate control signals via lines **232** such as user read/write strobes. Illustratively, the user read/write strobes control the writing of data from DTDM frames in the framer unit into associated FIFOs or other buffers. If the FIFO has byte wide format, the parallel output **206** may be used for this purpose. The delay unit **230** is used to insure that the necessary signal processing takes place before the DTDM frame leaves the framer unit.

7. Conclusion

A framer circuit for use in a network utilizing dynamic time division multiplexing has been disclosed. The framer circuit enables particular implementation of assemblers, disassemblers, multiplexers and demultiplexers suitable for a network utilizing dynamic time division multiplexing.

Finally, the above described embodiments of the invention are intended to be illustrative only. Numerous alternative embodiments may be devised by those skilled in the art without departing from the spirit and scope of the following claims.

What is claimed is:

1. A circuit comprising:
- a serial data input for receiving a data stream comprising frames,
- a serial-to-parallel converter for converting said frames to parallel form,
- a frame detector for detecting said frames in parallel form and for generating frame information,
- a control unit for receiving said information and for generating a control signal,
- a parallel data input for providing a parallel data stream,
- a tristate device operative under the control of said control signal for selectively enabling said parallel data stream, to be written into said frames in parallel form,
- a parallel-to-serial converter for reconverting said written parallel frames to serial form, and
- a serial data output by which said frames in serial form leave said circuit.

2. The circuit of claim **1** wherein said frames are DTDM frames.

3. A circuit for generating a bit stream comprising a chain of empty frames, said circuit comprising:
- memory means containing frame alignment information,
- a control unit,
- a tristate device operative under control of said control unit, said control unit being adapted to periodically transmit a signal to said tristate device to enable said frame alignment information to be periodically read out of said memory,
- a parallel-to-serial converter for periodically receiving said frame alignment information from said tristate device and for converting said frame alignment information to serial form to produce said bit stream comprising said chain of empty frames, and
- a serial data output coupled to said parallel-to-serial converter by which said bit stream is transmitted out of said circuit.

4. A circuit with peripheral circuitry comprising:
- a serial data input for receiving a data stream comprising a chain of frames,
- a serial-to-parallel converter for converting said frames to parallel form,
- a frame detector for detecting said frames in parallel form and for generating frame information,
- a control unit for receiving said information and for utilizing said received information to selectively generate control signals for controlling said peripheral circuitry, and
- a parallel data output by which data contained in said frames in parallel form is selectively transmitted to said peripheral circuitry.

5. The circuit of claim **4** wherein said peripheral circuitry comprises a buffer.

6. The circuit of claim **5** wherein said circuit further comprises a delay unit coupled to said frame detector for storing said frames while information received from said frames is processed by said control unit.

7. The circuit of claim **4** wherein said frames are DTDM frames.

8. A circuit comprising:

a serial data input,

a serial-to-parallel converter connected to said serial data input,

a frame detector connected to said serial-to-parallel converter,

a control unit adapted to receive information from said frame detector and to generate control signals,

a plurality of data sources,

a tristate device associated with each of said data sources,

a parallel-to-serial converter coupled to said tristate device, and

a serial data output connected to said parallel-to-serial converter by which data in serial form is able to leave said circuit,

said tristate devices being operable under control of said control signal to selectively enable data to be transmitted from said data sources to said parallel-to-serial converter.

9. The circuit of claim **8** wherein one of said data sources comprises a parallel data input.

10. The circuit of claim **8** wherein one of said data sources is a memory storing frame alignment information.

11. The circuit of claim **8** wherein said circuit further includes a delay unit coupled to an output of said frame detector.

12. The circuit of claim **8** wherein said circuit further includes a parallel data output coupled to an output of said frame detector.

13. The circuit of claim **8** wherein said circuit further includes a parallel data output.

14. A circuit comprising:

a serial-to-parallel converter for receiving an input data stream comprising serial frames, said serial-to-parallel converter converting said serial frames to parallel frames,

a frame detector for detecting and examining said parallel frames to generate frame information,

a means for generating control signals in correspondence to said information,

a tristate device for receiving said parallel frames from said frame detector,

a second tristate device for receiving a parallel data input stream comprising frames,

an enabling means, responsive to said means for generation and said tristate devices, for receiving said control signals and for selectively writing into said parallel frames said parallel data stream to produce completed frames, and

a parallel-to-serial converter for receiving said completed frames and converting said completed frames to a serial output data stream.

* * * * *

EXHIBIT 9

IN THE UNITED STATES DISTRICT COURT

IN AND FOR THE DISTRICT OF DELAWARE

- - -

BELL COMMUNICATIONS RESEARCH, INC., now TELCORDIA TECHNOLOGIES, INC.,	:	CIVIL ACTION
Plaintiff	:	
v.	:	
FORE SYSTEMS, INC.,	:	
Defendant	:	NO. 98-586 (JJF)

- - -

Wilmington, Delaware
Thursday, March 23, 2000
1:04 o'clock, p.m.

- - -

BEFORE: HONORABLE JOSEPH J. FARNAN, JR., U.S.D.C.J.

- - -

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- - -

sequence, a sequence of repeating frames. Each of the frames has a transmission overhead field in it that contains control information, such as timing control information used for frame alignment at the receiver.

Now, we show these as these black bars here (indicating). These black bar -- each of these bars denotes one byte of information, and you can see this PISO, parallel in, serial out, takes the byte-wide signal coming from the frame generator and converts it into a bit serial sequence. You see we've turned -- we turned the byte bars end to end on the transmission line, and they're going out in a bit serial sequence.

Okay. The transmission overhead field coming out of the frame generator is followed by a payload field. And when the frame generator generates the payload field, it puts what we call empty byte data in it. It's bit values that represent like just zeros, which indicate the absence of packet information in that payload field.

So let's illustrate how DTDM works by turning this on.

Okay. Now, we have it running, and we see the source devices generating digital information coming in at different rates. The video signal device is putting out the bottom stream. It's coming in at a high rate. There's an Ethernet packet source coming in the

middle source, which is the medium speed rate. Then we have a telephone line, called a T-1, generating its digits at a low rate.

What happens is that you can see, depending on the rate at which the data is coming into the system, it fills its packet buffer up quicker or faster or slower.

What we have within the framer circuit are a group of control gates. Okay. There's a control gate shown here as a door at the output of each of the packet buffers, and then there's a control gate at the output of the frame generator.

What the controller does to generate the output stream is it monitors the fill level of the packet buffers. When it sees a complete packet stored up in one of the buffers, it opens the buffer output door, closes the frame generator output door so that the stream of ever packet data is read out of the buffer and inserted into the payload field of the transmission steam and it displaces the empty packet bytes that would otherwise be in the stream coming out of the frame generator.

Okay. You see the frame generator is generating the gray bytes. Those are the empty data bytes. Then it generates the overhead bytes.

When a packet buffer fills up, you're going to see right now, the T-1 packet just got inserted. Now

to be inserted into a specified slot within the frame, what DTDM does is frees you up to take the packet from any source, whenever it's available, shoot it right into the stream and put it into any payload field, the one that happens to be playing out at that time.

Finally, the claim recites, for transmitting data from each of said sources at its own desired bit rate.

I explained that in connection with the animation.

Once again, we saw that the bit rate is preserved from the input because the rate at which the packet buffers fill up is dependent on that bit rate and that's preserved all the way through the stream to the output device.

Finally, the claim says for transmitting data from said plurality of sources simultaneously via said bit stream.

We've already covered that.

Okay. Let's go on.

If you look at Claim 3 and compare it to the language of Claim 1, Claim 3 is simply Claim 1 with the filling step broken into a packetizing step and an inserting step.

The terms used in the various method steps are essentially the same as what we've already described,

so we don't need to go through Claim 3 in any kind of detail.

Let's take a look at Claim 4.

Okay. Claim 4 is an apparatus claim, your Honor. It's written in means plus function form. Claim 4 is essentially an apparatus version of Claim 3. So I won't take the time. We don't need to go through it and explain all of the meaning -- the meaning of all the terms of all over -- all over again. I will, however, point out that in accordance with 112, Paragraph 6, you have -- we have to show that there's corresponding structure disclosed in the patent specification for each one of these means, and I'd like to quickly point out where that corresponding structure is shown. And it's all shown in Figure 12, or most of it is shown in Figure 12, which in the framer circuit.

All right. The generating means would include the control 210, the frame byte ROM 224 and the timing generator 229. Okay. That would be in the case of a one-stage framing circuit.

Now, in a two-stage framing circuit, where the empty frame stream is generated in the first stage and sent over to the second stage where it's inserted into the payload field. In that instance, the generating means for the empty frames would be, again,

EXHIBIT 10

FILED

SEP 9 4 32 PM '99

CLERK U.S. DISTRICT COURT
DISTRICT OF DELAWARE

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

BELL COMMUNICATIONS RESEARCH, INC. (now TELCORDIA TECHNOLOGIES, INC.)	)	
Plaintiff,	)	
v.	)	Civil Action No. 98-586 MMS
FORE SYSTEMS, INC.	)	
Defendant.	)	

PLAINTIFF, BELL COMMUNICATIONS RESEARCH, INC.'S REPLY BRIEF IN SUPPORT OF ITS CLAIM INTERPRETATION ANALYSIS AND IN OPPOSITION TO THE ERRONEOUS CLAIM INTERPRETATION ADVANCED BY DEFENDANT, FORE SYSTEMS, INC.

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Date: September 9, 1999

Although Fore's enablement argument, discussed above, is less than clear, Fore apparently contends that the term "*[f]illing the empty payload fields in said frames*" means that the term is limited to putting only a single packet into a payload field. As shown above, Fore's enablement argument is legally flawed and Fore offers no evidence that one skilled in the art would not be enabled by the '306 patent to put more than one packet into a single payload field.[10]

v. ***"such that data in packetized format from any of said sources is written into any available payload field of any of said frames"***

Here again, Fore wants the court, for non-infringement purposes, to construe the claims to require insertion of only a single packet in each frame so that systems that insert multiple packets per frame are not within the literal language of the claim. As shown above, importing details of the described embodiments into a claim, when the plain language of the claim does not so warrant, defies the basic rules of claim construction.

Claims 1 and 3 require each frame to have "an empty payload field." Frames that have several empty payload fields literally have "an empty payload field," as claimed. Fore's attempt to have the Court rewrite the claims to require each frame to have "one and only one empty payload field" must be rejected. Fore cites no authority that requires patents to describe every embodiment within the scope of the claims, because no such rule exists.[11] An applicant need not describe more than one embodiment of a broad claim to adequately support that claim. *Ethicon Endo Surgery, Inc. v. United States Surgical Corp.*, 93 F.3d 1572, 1582 (Fed. Cir. 1996).

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[10] Fore simply ignores the fact that, during prosecution of the application leading to the '306 patent, the applicants explained to the Examiner that the invention would cover implementations having multiple packets in a single frame payload. Ex. 6 at A*82.

[11] Fore's argument (Brief, p. 13) that the '306 patent does not enable placing multiple packets in a frame is irrelevant. Claims 1 and 3 do not claim a process for inserting multiple packets in a frame. The claim language is nonetheless broad enough to cover a system that inserts more than one packet in each frame.

EXHIBIT 11

H
Only the Westlaw citation is currently available.

United States Court of Appeals,
Federal Circuit.
BICON, INC., and DIRO, INC., Plaintiffs-Appellants,
v.
THE **STRAUMANN** COMPANY and INSTITUT **STRAUMANN** AG, Defendants-Appellees.
No. 05-1168.

March 20, 2006.

Background: Owner of patent for apparatus used with dental implants sued competitor for infringement. The United States District Court for the District of Massachusetts, George A. O'Toole, Jr., J., 2004 WL 2387277, granted summary judgment of noninfringement, and owner appealed.

Holding: The Court of Appeals, Bryson, Circuit Judge, held that patent was not infringed.
Affirmed.

[1] Patents 165(4)

291k165(4) Most Cited Cases
Abutment structure described in preamble of patent claim for dental implant emergence cuff was integral part of claim, which added limitations to invention; preamble gave detailed description of abutment's physical characteristics and defined cuff in manner that depended on those physical characteristics.

[2] Patents 157(1)
291k157(1) Most Cited Cases
Patent claim is interpreted with eye toward giving effect to all terms in claim.

[3] Patents 165(4)
291k165(4) Most Cited Cases
Patent claim preamble language that merely states purpose or intended use of invention is generally not treated as limiting scope of claim.

[4] Patents 165(4)
291k165(4) Most Cited Cases
There is no litmus test for determining whether patent claim preamble language is limiting.

[5] Patents 165(4)
291k165(4) Most Cited Cases
Whether to treat patent claim preamble as claim limitation is determined on facts of each case in light of claim as a whole and invention described in patent.

[6] Patents 165(4)
291k165(4) Most Cited Cases
Disregarding
If body of patent claim sets out complete invention, preamble is not ordinarily treated as limiting scope of claim; however, preamble is regarded as limiting if it recites essential structure that is important to invention or necessary to give meaning to claim.

[7] Patents 165(4)
291k165(4) Most Cited Cases
When limitations in body of patent claim rely upon and derive antecedent basis from claim preamble, then preamble may act as necessary component of claimed invention.

[8] Patents 236(2)
291k236(2) Most Cited Cases
Patent for dental implant emergence cuff, to be used in connection with specifically shaped implant abutment, was not literally infringed by accused devices designed to fit on differently shaped abutments.
[9] Patents 237
291k237 Most Cited Cases
Patent for dental implant emergence cuff, to be used in connection with implant abutment having convex, frusto-spherical basal surface, was not equivalently infringed by accused devices designed to fit on concave, trumpet-shaped abutments.

[10] Patents 226.7
291k226.7 Most Cited Cases
Patent claim that contains detailed recitation of structure is properly accorded correspondingly limited recourse to doctrine of equivalents.

[11] Patents 286
291k286 Most Cited Cases
Exclusive licensee may sue on patent, if patent owner is joined as party, but nonexclusive licensee may not.

[12] Patents 286
291k286 Most Cited Cases
Nonexclusive patent license was not rendered exclusive, such as would give licensee standing to sue for infringement, merely because licensee was patentee's sole current licensee.

Patents 328(2)
291k328(2) Most Cited Cases
5,749,731. Cited.
Appealed from: United States District Court for the District of Massachusetts. Judge George A. O'Toole, Jr.

Frank P. Porcelli, Fish & Richardson P.C., of Boston, Massachusetts, argued for plaintiffs-appellants. With him on the brief were Charles Hieken and Thomas A. Brown. Of counsel were Colter Paulson, Fish & Richardson P.C., of Boston, Massachusetts; and Berj A. Terzian, of Newbury, Massachusetts.

Milton Sherman, Kaye Scholer LLP, of New York, New York, argued for defendants-appellees. Of counsel was Stephen J. Elliott.

Before MICHEL, Chief Judge, BRYSON, and GAJARSA, Circuit Judges.

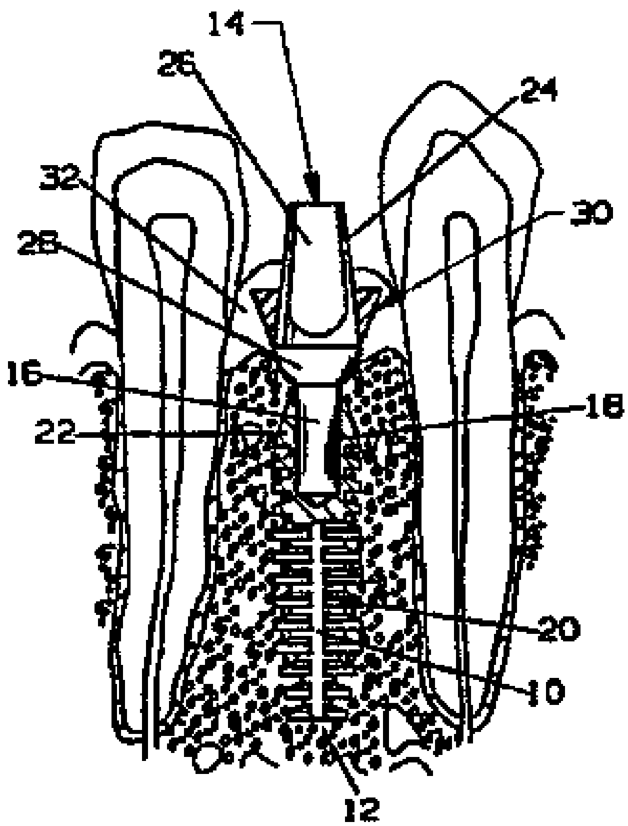
BRYSON, Circuit Judge.

***1** This case turns on the construction of a patent that claims an apparatus used with dental implants. The patent, U.S. Pat. No. 5,749,731 ("the '731 patent"), describes a plastic cuff that is designed to preserve a space around a dental implant so that when a dental crown is placed on top of the implant, the base of the crown can fit beneath the patient's gum line.

Diro, Inc., owns the '731 patent. Joined by its licensee (Bicon, Inc.), Diro sued The Straumann Company and Institut Straumann AG (collectively, "Straumann") for patent infringement based on Straumann's sale of two devices that are used in the preparation of crowns for dental implants. The United States District Court for the District of Massachusetts granted Straumann's motion for summary judgment of noninfringement and dismissed Bicon as a party plaintiff for lack of standing. *Bicon, Inc. v. The Straumann Co.*, Civil Action No. 01-10269 (D.Mass. Nov. 16, 2004). We affirm.

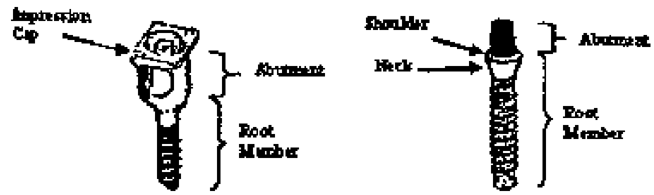
I

A dental implant prosthesis of the type described by the patent has two separate parts--the root member or implant, which is implanted in the patient's jaw bone and secures the device in place (number 10 in the figure below, which is Fig. 1 of the '731 patent); and the head member or abutment, which attaches to the root member and sticks up above the patient's gum line to provide the structure for attaching a crown (number 14 in the figure below). *See* '731 patent, col. 1, ll. 18-23. The '731 patent explains that after the patient's jaw and mouth heal from the surgery to implant the root member, the permanent abutment member is mounted on the root member. Because gum tissue "tends to heal taut to the head of the abutment member so that when the permanent crown is placed on the abutment member the margin of the crown is not concealed," *id.*, col. 2, ll. 6-9, the patent describes using the claimed emergence cuff (number 30 in the figure below) to keep the gum from closing around the abutment while the patient's jaw and mouth continue to heal. When the healing process is complete, the dentist can remove the cuff and can take advantage of the space left by the cuff to affix the permanent crown to the abutment at a point beneath the patient's gum line. Securing the permanent crown below the gum line has the cosmetic advantage of preserving the natural look of the patient's gum line with the crown installed. *Id.*, col. 2, ll. 5- 63; col. 3, ll. 61-64. In addition, use of the cuff enables the dentist to bond a temporary crown to the cuff at the time it is placed on the abutment, while the permanent crown is being prepared. *Id.*, col. 2, ll. 65-67.



In the complaint, Diro and Bicon (collectively, "Diro") alleged that Straumann had infringed at least claim 5 of the '731 patent by manufacturing, using, selling, and offering to sell products that incorporated the subject matter of the claims. In the course of the litigation, Diro identified two Straumann products that are used with dental implants as the allegedly infringing devices.

***2** The first device, called an "impression cap," is a plastic device that attaches to the shoulder portion of the root member in Straumann's system while the dentist is taking a mold that is used to prepare the crown that is to be fitted on the abutment. The impression cap is the superstructure that fits over the abutment and the shoulder of the root member while the mold for the crown is being taken. The impression cap is removed as soon as the mold is completed, a process that takes only a few minutes. The first figure below depicts the Straumann impression cap fitted over the Straumann abutment and attached to the shoulder of the Straumann root member. The second figure depicts the Straumann root member with the shoulder and neck portions designated.



The second device, called a "burnout coping," is a cone-shaped plastic structure that is used in fabricating the permanent crown. The burnout coping is never placed in the patient's mouth, but instead is used in the laboratory in the process of constructing the crown. It fits over a device known as the analog, which has the same shape as the abutment and shoulder portion of the root member in the patient's mouth. The figure below depicts the Straumann burnout coping.

Claim 5 of the '731 patent provides as follows (in reproducing the claim, we have subdivided it so as to facilitate reference to different portions of the claim):

An emergence cuff member for use in preserving the interdental papilla during the procedure of placing an abutment on a root member implanted in the alveolar bone of a patient in which

[a] the abutment has a frusto-spherical basal surface portion and

[b] a conical surface portion having a selected height extending therefrom comprising

[c] a generally annular member formed of biocompatible synthetic plastic having first and second ends,

[d] a bore extending from the first to the second ends,

[e] the bore having a taper generally matching that of the conical surface portion of the abutment,

[f] the larger end of the bore being at the first end,

[g] the outer surface of the annular member forming a feathered edge with the bore at the first end of the annular member,

[h] the distance between the first and second ends being less than the height of the conical surface,

[i] the diameter of the cuff member increasing in the direction going from the first end to the second end, and

[j] a radially inwardly extending flexible lip formed at the

first end of the cuff member.

After construing the claim, the district court granted summary judgment of noninfringement to Straumann on several grounds. First, the court concluded that the lengthy preamble of claim 5 (the portion from the beginning of the claim through part [b]) is an integral part of the claim and limits the claim. The court then held that one of the limitations in the preamble--an abutment having a frusto-spherical basal surface portion--is not satisfied by either of the accused devices.

***3** Second, the court held that the Straumann impression cap and burnout coping do not have the structure recited in part [e] of the claim. With respect to the impression cap, the court held that the taper of the portion of the cap at issue matches the shoulder portion of the root member in the Straumann system, not the conical surface of the abutment. With respect to the burnout coping, the court noted that while the taper of the upper portion of the internal bore in the Straumann burnout coping generally matches the taper of the conical outer surface of the Straumann abutment, Diro's infringement argument rested on the contention that it was the lower portion of the burnout coping that constituted the claimed annular member. The taper of the bore in that portion of the burnout coping, the court explained, matches the taper of the shoulder of the root member, not the taper of the abutment.

Third, the court held that part [h] of the claim does not read on the accused devices because the distance between the first and second ends of the annular member in the impression cap and burnout coping is not less than the height of the conical surface of the abutment. Finally, the court ruled that part [i] of the claim does not read on the burnout coping, because the burnout coping does not contain any structure consisting of an annular member with a diameter that is greater at the second end than at the first.

The court further held that the complaint had to be dismissed as to plaintiff Bicon, Inc., for lack of standing. Although Bicon claimed to be a licensee of Diro's patent, the court held that the evidence proffered in the course of the summary judgment proceedings did not justify a finding that Bicon had an exclusive license to the patent. As a mere nonexclusive licensee, the court held, Bicon was not entitled to sue for infringement of the patent, even as a co-plaintiff with the patent owner, Diro.

II

A

[1] Claim 5 of the '731 patent is a difficult claim to make sense of. Despite the claim's detailed description of and references to an abutment, in Diro's view the claim is in no way limited by the abutment. Diro's argument in support of that construction boils down to two fundamental contentions. First, Diro points out that the claim recites "[a]n emergence cuff member," not a combination consisting of an emergence cuff member and other features, such as an abutment having certain specific characteristics. Second, Diro assigns critical significance to the fact that the abutment's description is in the preamble of the claim--the preamble consisting of everything in the claim preceding the word "comprising," including what we have labeled as parts [a] and [b]. The preamble, Diro argues, in no way limits the claim because it merely sets forth the purpose or use of the emergence cuff. Accordingly, Diro characterizes claim 5 as encompassing any device having the structure of the annular member recited in the body of the claim that is capable of cooperating with any abutment.

***4** The problem with Diro's argument is that, because claim 5 includes a detailed description of the abutment's physical characteristics and defines the emergence cuff in a way that depends on those physical characteristics, the invention that is recited in claim 5 and described in its supporting specification can only be understood as being limited by the abutment recited in the claim. Together, the preamble and the body of the claim contain a detailed description of the features of the abutment used in connection with the emergence cuff. The preamble states that the abutment has "a frusto-spherical basal surface portion and a conical surface portion having a selected height extending therefrom." The body of the claim states that the internal bore of the emergence cuff has "a taper generally matching that of the conical surface portion of the abutment." The body adds that "the distance between the first and second ends [of the emergence cuff is] less than the height of the conical surface" of the abutment. For several reasons, that

detailed recitation of the features of the abutment is incompatible with Diro's theory that the claim concerns only the features of the emergence cuff and that the references to the abutment merely describe the intended use of the emergence cuff.

First, the requirement that the cooperating abutment have "a frusto-spherical basal surface portion" would have no meaning if the claim were limited to the structure of the emergence cuff. Diro argues that the claim requires only that the emergence cuff "interoperate with an abutment that does contain such an element." But nothing in Diro's argument suggests how the shape of the basal surface portion of the abutment has any effect on the required structure of the emergence cuff. If there is no such effect, then under Diro's proposed claim construction the recited "frusto-spherical basal surface portion" of the abutment has no role in the claim and thus is entirely superfluous.

[2] The purpose of a patent claim is to define the precise scope of a claimed invention, thereby "giv[ing] notice both to the examiner at the U.S. Patent and Trademark Office during prosecution, and to the public at large, including potential competitors, after the patent has issued." *Johnson & Johnston Assocs., Inc. v. R.E. Serv. Co.*, 285 F.3d 1046, 1052 (Fed.Cir.2002) (en banc). Allowing a patentee to argue that physical structures and characteristics specifically described in a claim are merely superfluous would render the scope of the patent ambiguous, leaving examiners and the public to guess about which claim language the drafter deems necessary to his claimed invention and which language is merely superfluous, nonlimiting elaboration. For that reason, claims are interpreted with an eye toward giving effect to all terms in the claim. *See, e .g., Elekta Instrument S.A. v. O.U.R. Scientific Int'l, Inc.*, 214 F.3d 1302, 1305, 1307 (Fed.Cir.2000) (claim language "only within a zone extending between latitudes 30°-45°" does not read on a device with radiation sources extending between 14° and 43° because "[a]ny other conclusion renders the reference to 30° superfluous"); *Unique Concepts, Inc. v. Brown*, 939 F.2d 1558, 1563 (Fed.Cir.1991) ("When the language of a claim is clear, as here, and a different interpretation would render meaningless express claim limitations, we do not resort to speculative interpretation based on claims not granted."); *In re Danly*, 46 C.C.P.A. 792, 263 F.2d 844, 847 (CCPA 1959) (limiting claims to require that the claimed device actually be connected to an alternating current source because, although the claims "do not positively recite a source of alternating current as an element of the claims," any other interpretation would render certain language in the claims meaningless). If we were to accept Diro's arguments, we would be requiring the public to look past the plain language of the claims and guess whether a detailed description of a structural feature in a claim is superfluous to the scope of the claimed invention and unnecessary to establish infringement.

***5** The second problem with Diro's argument is that if the claim reads on any hypothetical abutment, limitations [e] and [h] are rendered meaningless. If the claim limitations include only those elements of the claim that pertain to the structural features of the emergence cuff, as Diro contends, the requirement that "the distance between the first and second ends [of the emergence cuff must be] less than the height of the conical surface" of the abutment would make no sense. Since the abutment, in Diro's view, refers to any abutment that could cooperate with the emergence cuff, the height limitation would never exclude any device. No matter what the distance between the first and second ends of the emergence cuff in question, an abutment could always be hypothesized that would have a height greater than that distance. Thus, Diro's claim construction would read the height limitation out of the claim altogether.

Similarly, if the claim is construed to include any hypothetical abutment that could cooperate with the emergence cuff, the requirement that the bore of the emergence cuff have a taper "generally matching that of the conical surface portion of the abutment" would be meaningless. That is because an abutment could always be hypothesized that would have a taper matching the taper of the bore of any emergence cuff. The "matching taper" limitation would therefore be reduced to requiring only that the bore of the emergence cuff have a taper.

In sum, the effect of adopting Diro's proposed claim construction would be to read limitations [a], [b], [e], and [h] out of the claim. Not only would that be contrary to the principle that claim language should not treated as

meaningless, but it would be contrary to the specification, which describes the features of the claimed abutment in detail, not only in the description of the preferred embodiments, but in the background and summary of the invention portions of the specification as well. *See* '731 patent, col. 1, ll. 43-51 (the abutment "has an upstanding generally tapered, conical exterior surface with an anti-rotational flat surface portion for mounting the prosthetic crown and a basal portion having a convex, frusto-spherical exterior surface which extends downwardly from the tapered portion"); col. 2, ll. 47-53 (tapered bore of the cuff matches that of the conical surface portion of the abutment, "i.e., a taper generally approximately 7 degrees," with the feathered edge of the cuff "adapted to serve as a smooth continuation of the frusto-spherical surface of the basal portion of the abutment"); col. 3, ll. 44-54 (the abutment "has an upstanding, generally tapered, conical surface ... with an anti-rotational flat surface ... for mounting a prosthetic crown and a basal portion ... having a convex, frusto-spherical exterior surface which extends downwardly from the tapered portion"); col. 4, ll. 3-14 (referring to the diameter of the frusto-spherical portion and the taper of the conical surface portion of abutments typically used with the emergence cuff).

***6** In light of the problems presented by Diro's proposed construction, we conclude that the correct construction of claim 5 of the '731 patent is the one adopted by the district court, in which the claim is treated as one to an emergence cuff when used in conjunction with an abutment having the features recited in the claim. Despite the fact that the claim begins with a reference to the emergence cuff alone, the full text of the claim, read in the context of the entire patent, indicates that the claimed invention is the combination of the emergence cuff and the abutment, operating together in the fashion recited in the claim and described in the specification.

Diro's second and related argument in support of its proffered construction is that the abutment's features are described in the preamble, so the only way to limit claim 5 according to those features is to treat the preamble as limiting the claim. To so limit the claim, Diro argues, would violate the principles of this court's decisions governing the role of preamble language in claim construction. Again, we disagree.

[3][4][5] While it is true that preamble language is often treated as nonlimiting in nature, it is not unusual for this court to treat preamble language as limiting, as it is in this case. Preamble language that merely states the purpose or intended use of an invention is generally not treated as limiting the scope of the claim. *See* *Boehringer Ingelheim Vetmedica, Inc. v. Schering-Plough Corp.*, 320 F.3d 1339, 1345 (Fed.Cir.2003); *Rowe v. Dror*, 112 F.3d 473, 478 (Fed.Cir.1997). However, we have stated that there is no "litmus test" for determining whether preamble language is limiting. *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed.Cir.2002). To the contrary, we have stated that "whether to treat a preamble as a claim limitation is determined on the facts of each case in light of the claim as a whole and the invention described in the patent." *Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 831 (Fed.Cir.2003).

[6][7] If the body of the claim "sets out the complete invention," the preamble is not ordinarily treated as limiting the scope of the claim. *Schumer v. Lab. Computer Sys., Inc.*, 308 F.3d 1304, 1310 (Fed.Cir.2002). However, the preamble is regarded as limiting if it recites essential structure that is important to the invention or necessary to give meaning to the claim. *NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1305-06 (Fed.Cir.2005), *cert. denied,* 74 U.S.L.W. 3421 (U.S. Jan. 23, 2006); *SanDisk Corp. v. Memorex Prods., Inc.*, 415 F.3d 1278, 1284 n. 2 (Fed.Cir.2005), *cert. denied,* --- U.S. ----, 126 S.Ct. 829, 163 L.Ed.2d 707 (2005). That is, if the claim drafter "chooses to use *both* the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." *Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp.*, 55 F.3d 615, 620 (Fed.Cir.1995) (emphasis in original). Moreover, when the limitations in the body of the claim "rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed.Cir.2003).

***7** We conclude, as did the district court, that the preamble

to claim 5 of the '731 patent recites essential elements of the invention pertaining to the structure of the abutment that is used with the claimed emergence cuff. First, as we have noted, the preamble of claim 5 is not limited to stating the purpose or intended use of the invention, but contains structural features of the abutment. Moreover, the body of the claim does not recite the complete invention, but refers back to the features of the abutment described in the preamble, so that the references to the abutment in the body of the claim derive their antecedent basis from the preamble. And because the preamble recites structural features of the abutment, it is apparent that the claim drafter chose to use both the preamble and the body of the claim to define the subject matter of the claimed invention. Indeed, as described above, if claim 5 is not limited to the particular abutment described in the preamble, limitations [e] and [h] of claim 5 become meaningless.

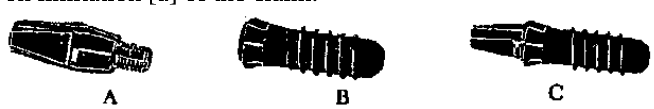
In arguing that no part of the preamble limits the scope of claim 5, Diro relies on language from the lead opinion in *C.R. Bard, Inc. v. M3 Systems, Inc.*, 157 F.3d 1340 (Fed.Cir.1998). The claim that was at issue in that case, however, is quite different from the claim at issue here. The preamble in *Bard* described a biopsy needle for use with a tissue sampling device; the device was described as having a housing with two slides to permit longitudinal motion. The body of the claim recited a hollow first needle with a head for coupling the needle to the first slide and a second needle extending through the first needle and having a head for coupling to the second slide. The opinion in *Bard* explained that the preamble merely described the portion of the housing necessary to define the intended function of the needles that were the subject of the claim. 157 F.3d at 1350. In this case, by contrast, the preamble recites structure for the abutment that goes well beyond what is necessary to describe the intended purpose of the emergence cuff. The recitations of the "frusto-spherical basal surface" of the abutment and the height of the conical surface of the abutment do not serve to describe the function of the emergence cuff, but instead are necessary to define the structure of the claimed device. Accordingly, the analysis in *Bard* is not at odds with our conclusion, and that of the district court, that the preamble incorporates limitations relating to the abutment.

B

After determining that the recited features of the abutment are part of claim 5 of the '731 patent, the district court concluded that the accused impression caps and burnout copings do not infringe. Although we do not address all the grounds on which the district court based its noninfringement ruling, we agree that the accused devices do not infringe, either literally or under the doctrine of equivalents.

1

[8] With regard to literal infringement, we sustain the district court's decision on two grounds. First, as the district court explained, neither of the Straumann devices is used in connection with an abutment having a convex, frusto-spherical basal surface portion, because the basal surface portions of the abutments used in the Straumann system do not have a convex frusto-spherical shape. Although Diro argues that the frusto-spherical basal surface portion of the abutment can be either concave or convex, the written description makes clear that the frusto-spherical basal surface portion was intended to be convex, not concave, as the terms "frusto-spherical" basal surface portion and "convex, frusto-spherical" basal surface portion are used interchangeably in the written description. *See* '731 patent, col. 1, ll. 46, 48-49; col. 2, ll. 52-53; col. 3, ll. 47-48, 49-50. The convex frusto-spherical basal surface portion of the abutment of the '731 patent is depicted as number 28 in figure 1 from the patent, reproduced above. Even if the term "frusto-spherical" were interpreted to encompass concave structures, the term would still not read on the Straumann abutment, because the basal portion of the Straumann abutment does not form a portion of a sphere, either convex or concave. Instead, the basal portion of the Straumann abutment has a frusto-conical surface, as shown in the figures below, which depict the Straumann abutment (A), the Straumann root member (B), and the two affixed together (C). The Straumann devices therefore do not read on limitation [a] of the claim.



***8** Second, the Straumann devices do not satisfy limitation [e] of claim 5, because the taper of the pertinent portion of

the internal bore of the Straumann devices matches the taper of the shoulder portion of the Straumann root member, not the taper of the Straumann abutment. Diro does not contend that the taper of the bore in the Straumann impression cap and burnout coping matches the taper of the Straumann abutment. Rather, Diro argues that "[s]o long as the caps and copings have bores with a taper that generally matches the conical surface portion of *an* abutment, the devices infringe" (emphasis in original). In other words, Diro reads limitation [e] as encompassing any device that has a taper matching the taper of any conical surface that could be found on any device that could serve as an abutment. The problem with that argument is that "the abutment" of limitation [e] refers to the particular abutment described in the preamble of the claim, not to any structure that could conceivably serve as an abutment. Claim 5 clearly distinguishes between the abutment and the root member, as the district court held. Thus, for the purposes of limitation [e] we must look to the taper of Straumann's abutment, not the taper of some other structure such as Straumann's root member. Because Straumann's bores do not match the taper of Straumann's abutment, the devices do not satisfy limitation [e].

Diro argues that when Straumann's root member and abutment are screwed together they constitute a single structure, and that the abutment and the shoulder portion of the root member should be viewed as constituting the abutment of claim 5. Thus defined, the abutment would have two conical surfaces, one corresponding to the shoulder of Straumann's root member, and one corresponding to Straumann's abutment. Even if we were to accept that argument, the specification clearly shows that the conical surface referred to in claim 5 is what the patent abstract refers to as the "crown receiving surface of the abutment." *See* '731 patent, col. 2, ll. 47-50 ("The cuff has a tapered bore essentially matching that of the crown mounting conical portion of the abutment member, i.e., a taper generally approximately 7 degrees ...."). That conical surface, the specification notes, "has a taper of approximately 7 degrees," *id.,* col. 4, ll. 6-7, and an "anti-rotational flat surface ... for mounting a prosthetic crown," *id.,* col. 3, ll. 45-46. In the Straumann system, the crown is mounted on the abutment, which is tapered to approximately 7 degrees and has an anti-rotational flat surface; the shoulder of Straumann's root member, however, has a taper of approximately 45 degrees and no anti-rotational flat surface on which a permanent crown is mounted. Although claim 5 is not limited to any particular angle or anti-rotational flat surface, the specification, the drawings, and the language of claim 5 clearly show that claim 5 references the sort of conical surface found on Straumann's abutment, not the sort found on Straumann's root member. In other words, the patent calls for a bore that matches the taper of a particular conical surface, not merely a bore that matches the taper of any conical surface found in the dental implant system. For that reason as well, Straumann's devices do not literally infringe claim 5 of the '731 patent.

2

***9** [9] With regard to infringement under the doctrine of equivalents, we again concur in the district court's analysis. We hold that the district court correctly rejected Diro's theory that the trumpet-shaped surface of the neck of Straumann's root member, which Diro characterizes as concave, is equivalent to the convex, frusto-spherical basal surface of the abutment that is described in the '731 patent. As the district court noted, Diro's theory--that a concave structure on the root member is equivalent to a convex structure on the abutment--would be at odds with the claim limitation requiring that the basal surface portion of the abutment be frusto-spherical in shape.

[10] The problem that Diro faces in this regard is that limitations [a] and [b] of the claim contain a detailed recitation of the shape of the abutment, including that it has a frusto-spherical basal portion. A claim that contains a detailed recitation of structure is properly accorded correspondingly limited recourse to the doctrine of equivalents. *See* *Tanabe Seiyaku Co. v. Int'l Trade Comm'n,* 109 F.3d 726, 732 (Fed.Cir.1997) ("The sharply restricted nature of the claims has much to do with the scope we accord to the doctrine of equivalents."). That principle has special application in a case such as this one, where the claim recites a particular shape for the basal portion of the abutment that clearly excludes distinctly different and even opposite shapes. In such cases, we have explained, "by

defining the claim in a way that clearly excluded certain subject matter, the patent implicitly disclaimed the subject matter that was excluded and thereby barred the patentee from asserting infringement under the doctrine of equivalents." *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1346 (Fed.Cir.2001); *see also* *Asyst Techs., Inc. v. Emtrak, Inc.*, 402 F.3d 1188, 1195 (Fed.Cir.2005) ("To hold that 'unmounted' is equivalent to 'mounted' would effectively read the 'mounted on' limitation out of the patent."); *Moore U.S.A., Inc. v. Standard Register Co.*, 229 F.3d 1091, 1106 (Fed.Cir.2000) ("[I]t would defy logic to conclude that a minority--the very antithesis of a majority--could be insubstantially different from a claim limitation requiring a majority, and no reasonable juror could find otherwise."); *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1160 (Fed.Cir.1998) (to hold that a device with a hemispherical shape infringes a patent requiring that the device have a "generally conical outer surface" would "write the 'generally conical outer surface' limitation out of the claims"); *Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 149 F.3d 1309, 1317 (Fed.Cir.1998) (subject matter is "specifically excluded" from coverage under the doctrine of equivalents if its inclusion is "inconsistent with the language of the claim").

Both of the structures in the Straumann system that are possible candidates for equivalence to the abutment base recited in the claim fall victim to this principle of specific exclusion. As we have noted, the basal portion of the Straumann abutment is frusto-conical, not frusto-spherical, and the neck of the Straumann root member is concave, not convex. Those shapes are clearly contrary to, and thus excluded by, the patentee's characterization of its abutment as having a convex, frusto-spherical shape. For that reason, neither the basal portion of the Straumann abutment nor the neck of the Straumann root member can be equivalent to the convex frusto-spherical basal surface portion of the abutment recited in limitation [a].

***10** With respect to limitation [e], Diro essentially argues that the conical top portion of the shoulder of the Straumann root member is equivalent to the conical surface portion of the claim 5 abutment, and therefore that the taper of Straumann's bores is equivalent to the taper required by the claim. We disagree. Diro's equivalence argument would read the taper limitation out of the claim because it would expand the scope of that limitation to encompass any taper that matches any conical surface in the system. As discussed above, limitation [e] of the claim explicitly refers to the abutment that is described in the preamble, and the specification shows that the relevant conical surface is that of the Straumann abutment, not that of the Straumann shoulder. Accordingly, we agree with the district court that Straumann's devices do not infringe, either literally or under the doctrine of equivalents, and we uphold the court's decision granting Straumann's motion for summary judgment of noninfringement.

III

[11] Bicon appeals from the order of the district court dismissing it as a party on the ground that, as a nonexclusive licensee of the '731 patent, it lacked standing to sue for infringement of the patent. The parties do not disagree over the proposition that an exclusive licensee may sue on a patent, if the patent owner is joined as a party, but that a nonexclusive licensee may not. *See* *Schreiber Foods, Inc. v. Beatrice Cheese, Inc.*, 402 F.3d 1198, 1202-03 (Fed.Cir.2005); *Ortho Pharm. Corp. v. Genetics Inst., Inc.*, 52 F.3d 1026, 1031 (Fed.Cir.1995). Instead, what divides the parties is that Bicon argues that it was an exclusive licensee to the '731 patent, while the district court found, and Straumann argues, that Bicon's license under the patent was nonexclusive.

The district court held that it was uncontroverted that Bicon was a nonexclusive licensee of the '731 patent. Bicon argues, however, that there was a genuine issue of material fact before the district court as to the nature of Bicon's license and that the issue was therefore not one that the district court was entitled to resolve on summary judgment.

[12] We have examined the record references cited by Bicon in support of its contention that its license to the '731 patent was exclusive, and we conclude, as did the district court, that the record does not support Bicon's argument. The only evidence Bicon cites in support of its contention that its license was exclusive is the testimony of its president, Dr. Vincent Morgan. Dr. Morgan testified that Bicon's right to

practice the patent was "exclusive at the moment," but he promptly explained that Bicon's right to practice the patent was "exclusive" only in the sense that Bicon was the only licensee of the Diro patent at the time ("[I]t's exclusive because Bicon is the only one doing it right now."). He added that he was aware of nothing that would prevent Diro "from licensing [the patent] to someone else under appropriate circumstances." We conclude that Bicon failed to proffer any evidence that Bicon was an exclusive licensee with the right to exclude other prospective licensees and in that capacity had standing to bring suit for infringement of the '731 patent. We therefore uphold the district court's ruling on the standing issue.

AFFIRMED.

--- F.3d ----, 2006 WL 688797 (Fed.Cir.(Mass.))

END OF DOCUMENT

EXHIBIT 12

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/152,238	02/04/88	LAU C	1

JAMES W. FALK
BELL COMMUNICATIONS RESEARCH, INC.,
290 WEST MOUNT PLEASANT AVE.
LIVINGSTON, NJ 07039

EXAMINER	
CHIN,W	
ART UNIT	PAPER NUMBER
263	3

DATE MAILED: 10/06/88

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on ______ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ___ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☒ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of informal Patent Application, Form PTO-152
5. ☒ Information on How to Effect Drawing Changes, PTO-1474
6. ☒ List of Bonded Draftsmen

Part II SUMMARY OF ACTION

1. ☒ Claims 1-8 are pending in the application.
   Of the above, claims ______ are withdrawn from consideration.
   ______ have been cancelled.
2. ☐ Claims ______ are allowed.
3. ☐ Claims ______ are rejected.
4. ☒ Claims 1-8 are objected to.
5. ☐ Claims ______ are subject to restriction or election requirement.
6. ☐ Claims ______
7. ☒ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on ______. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on ______ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed ______, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. ______; filed on ______.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

Serial No. 152,238

Art Unit 263

1. The drawings are objected to because the figures lack descriptive labels. Correction is required.

2. Applicant is required to submit a proposed drawing correction in response to this Office action. However, correction of the noted defect can be deferred until the application is allowed by the examiner.

3. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, page 8, lines 10-11, "the improved node" lacks antecedent basis. Claim 1, page 8, line 12, it is unclear what "the rings" is referring to, as there is no clear antecedent for this terminology.

Claim 1, page 8, lines 14 and 20 respectively, it is unclear what structure "the associated rings" is referring to. Claim 4, page 9, lines 6-7, it is unclear what "the associated rings" are, as it is unclear as to what the rings are being associated with and there is no clear antecedent for a first and second ring only. Claim 4, page 9, lines 10-11, it is unclear if "a corresponding receiver" is meant to refer to one of the subrate receivers previously recited. Claims 5-8 are rejected for similar reasons as those set forth above.

4. Claims 1-8 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. 112.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Prior art cited is typical of prior fault recovery tech-

Serial No. 152,238

Art Unit 263

niques used in multiple ring communication systems.

6. Any inquiry concerning this communication should be directed to Wellington Chin at telephone number 703-557-3374.

W. Chin:vj

703-557-3374

10-03-88 *Kl*

Douglas W. Olms

DOUGLAS W. OLMS
PRIMARY EXAMINER
GROUP 263

EXHIBIT 13

MAIL ROOM JAN 6 1989 PAT. & TRADEMARK OFF.

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Chi-Leung Lau
Case 1
Serial No. 152,238 Filed February 4, 1988
Group Art Unit 263
Examiner W. Chin
Title Survivable Ring Network

RECEIVED
JAN 10 1989
GROUP 260

THE COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, D. C. 20231

SIR:

In response to the Office action dated October 6, 1988 (application paper No. 3), please amend the above-identified application as follows:

IN THE SPECIFICATION

Page 5, line 1, replace "bold" with --dashed--.

IN THE CLAIMS

Please amend claims 1, 3, 4, 5, 7 and 8 as follows:

1. (Amended) In a communications network having a plurality of nodes interconnected in a ring configuration by a first ring which conveys multiplexed subrate communications around the first ring from node to node in one direction and a second ring which conveys multiplexed subrate communications around the second ring from node to node in the other direction, each node including subrate transmitters with associated multiplexers and demultiplexers with associated subrate receivers, an [the] improved node comprising

monitoring means, associated with the first ring and the second ring [rings], for evaluating the integrity of the multiplexed subrate communications on the first ring and the second ring, respectively [each of the associated

rings], and

A1

insertion means, associated with the demultiplexers and said monitoring means, for inserting an error signal on designated ones of the subrate communications in response to said monitoring means detecting a lack of integrity on the multiplexed subrate communications on the first ring or the second ring or both the first ring and the second ring [at least one of the associated rings].

3. (Amended) In the communications network of claim 1, the improved node wherein the multiplexers multiplex selected subrate communications containing said error signal into a multiplexed subrate communication for transmission onto the first ring or the second ring or both in correspondence to said detection of said error signal [the associated rings].

A2

4. (Amended) A communications network having a plurality of nodes interconnected in a ring configuration by a first ring which conveys multiplexed subrate communications around the first ring from node to node in one direction and a second ring which conveys multiplexed subrate communications around the second ring from node to node in the other direction, each of said nodes including subrate transmitters and subrate receivers and further comprising:

monitoring means, associated with the first ring and the second ring, for evaluating the integrity of the multiplexed subrate communications on the associated first ring and the associated second ring, respectively [each of the associated rings],

means for demultiplexing the multiplexed subrate communications on the associated first ring and the associated second ring into subchannels wherein at least one of said subchannels is sent to [a] one of the corresponding receivers [receiver],

insertion means associated with said demultiplexing means to insert an error signal on each of

said subchannels in response to said monitoring means detecting a lack of integrity on the multiplexed subrate communications on [one] the associated first ring or the associated second ring or both the associated first ring and the associated second ring [of the associated rings],

selector means associated with said demultiplexing means for selecting, in response to the detection of said error signal on one of the subchannels, one of the other subchannels, and

multiplexing means for multiplexing subchannels and inserting multiplexed subrate communications onto the associated first ring and the associated second ring, respectively.

5. (Amended) A communications network having a first grouping of nodes interconnected by a first ring arrangement, a second grouping of nodes interconnected by a second ring arrangement, each ring arrangement conveying multiplexed subrate communications in a first direction from node to node and conveying multiplexed subrate communications in a second direction from node to node, and each node includes [comprises] subrate transmitters with associated multiplexers and demultiplexers with associated receivers, and wherein

each node comprises

monitoring means, associated with [its] the ring arrangement connected to said each node, for evaluating the integrity of the multiplexed subrate communications on [the] said associated ring arrangement,

insertion means, associated with its demultiplexers and its monitoring means, for inserting an error signal on designated ones of said subrate communications in response to said monitoring means detecting a lack of integrity on said multiplexed subrate communications on its said associated ring arrangement, and

selector means, associated with its demultiplexers, for selecting, in response to the detection of said error signal on a subrate communication, a subrate

communication that does not contain an error signal, and

wherein a preselected node of the first ring arrangement comprises;

means, connected to the first ring arrangement and the second ring arrangement, for directing at least one subrate communication to the second ring arrangement and corresponding subrate communications from the second ring arrangement for multiplexing onto multiplexed subrate communications on the first ring arrangement.

7. (Amended) In a communications network having a plurality of nodes interconnected in a ring configuration by a first ring which conveys multiplexed subrate communications around the first ring from node to node in one direction and a second ring which conveys multiplexed subrate communications around the second ring from node to node in the other direction, each node including subrate transmitters with associated multiplexers and demultiplexers with associated receivers, an improved method associated with each node comprising the steps of

evaluating the integrity of the multiplexed subrate communications on the first ring and the second ring [each of said associated rings] with monitoring means associated with both the first ring and the second ring, and

inserting an error signal on designated ones of said subrate communications in response to said monitoring means detecting a lack of integrity on said multiplexed communications on the first ring or the second ring or both the first ring and the second ring [at least one of said associated rings].

8. (Amended) The method as recited in claim 7 further comprising the step of selecting, in response to the detection of said error signal on said at least one of the subrate communications, another of the subrate communications that does not contain an error.

Remarks

Claims 1-8 are pending in this application. As a result of the instant Office action, claims 1-8 stand rejected under 35 U.S.C. 112, second paragraph. However, the Examiner did indicate that claims 1-8 "would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. 112."

With respect to particular claims, the Examiner sets forth the following reasons as the basis for the rejection.

Claim 1

(a) "the improved node" on page 8, lines 10-11, lacks antecedent basis;

(b) on page 8, line 12, it is unclear what "the rings" is referring to, as there is no clear antecedent for this terminology; and

(c) on page 8, lines 14 and 20, respectively, it is unclear what structure "the associated rings" is referring to.

The Applicant has rewritten claim 1 to overcome the Examiner's reasons for rejecting claim 1. In particular, claim 1 now recites "an improved node" thereby indicating the first appearance of this structure in the claim. In addition, claim 1 now explicitly calls for "the first ring and the second ring" instead of "rings" so as to clarify the interrelationship among the various claim elements.

Claim 3, which is dependent on claim 1, has been amended to recite that the error signal is multiplexed for transmission onto "the first ring or second ring in correspondence to said detection of said error signal".

Claim 4

(a) on page 9, lines 6-7, it is unclear what "the associated rings" are, and it is unclear as to what the rings are associated with and there is no clear antecedent for the first and second ring only.

(b) on page 9, lines 10-11, it is unclear if "a corresponding

receiver" is meant to refer to one of the subrate receivers previously recited.

The Applicant has amended claim 4 in a manner similar to claim 1 in that the reasons for rejecting claim 4 are substantially the same used to reject claim 1. Claim 4 now calls for "the first associated ring" and "the second associated ring" in place of the less explicit term "rings".

Claims 5-8 have been rejected by the Examiner "for similar reasons for those set forth above" with respect to the rejections of claims 1 and 4. Accordingly, the Applicant has amended independent claims 5 and 7 in substantially the same manner as claims 1 and 4 to overcome the Examiner's rejections and place these claims in condition for allowance. In particular, claim 5 has been amended to clarify that each node has a monitoring means associated with the ring arrangement connected to each particular node and that the means for directing is connected to both the first ring arrangement and the second ring arrangement. With respect to claim 7, this claim now calls for "evaluating the integrity ... on the first ring and the second ring with monitoring means associated with both the first ring and the second ring", thereby clarifying any ambiguity in a manner commensurate with claim 1. Also, claim 8 has been amended for clarity in a manner commensurate with claim 2.

Finally, the drawing was objected to because (i) the figures lacked descriptive labels and (ii) bold black lines were used in FIG. 2 to differentiate lines carrying error signals from lines without error signals. The Applicant proposes that the bold lines in FIG. 2 be replaced with dashed lines, as shown on the enclosed, red-inked marked FIG. 2. The specification, on page 5, line 1, has been changed to reflect this change in FIG. 2. Does the Examiner concur with this proposed change? In addition, the Applicant requires guidance with respect to the objection on the basis that the figures lack descriptive labels. The Applicant has perused each FIGURE and believes all required descriptive labels/reference numerals have been clearly

identified, and there is correspondence among the specification, the drawing and the claims. If the Examiner believes correction is still required, would the Examiner please amplify on this remark and point out which FIGURES and the elements in these FIGURES that lack descriptive labels?

It is respectfully requested that claims 1-8 of this application be reconsidered and reexamined and that this application now passed to issue.

Respectfully submitted,
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Date: JAN 4 1989

Enclosure:
Red-inked marked FIG. 2